

# An RT-level Concurrent Error Detection Technique for Data Dominated Systems

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## Abstract

In this paper we present a Concurrent Error Detection (CED) technique that can be applied to behavioral RTL models of data dominated systems. The technique obtains CED through duplication of operations with shifted operands. Duplication is performed according to transformation rules that can automatically be applied to a behavioral model. Preliminary experimental results show the viability of the proposed technique.

## 1. Introduction

Some CED solutions for data dominated designs modeled as behavioral RT-level descriptions were recently proposed. In [1] the CED technique exploits idle clock cycles for replicating the model operations. Although the technique demands low area overhead, in the general case only partial coverage of all the faults affecting the circuit functional units (FUs) is achieved. In [2] a different approach is proposed based on re-computing (with changing operation-to-operator allocation or with shifted operands) of the algorithm the circuit implements. This approach allows to receive high coverage of the FUs faults, preserving low area overhead. As a drawback, it shows high time overhead or error detection latency.

Here we propose a CED technique which targets high coverage of the FUs faults (close to 100%). The checking of the FUs is fulfilled through recomputation of the design operations with shifted operands. The recomputation is carried out in the FUs implementing the normal computation of the design algorithm during idle clock cycles. In the case idle clock cycles are not enough for the duplication purposes the possibility of introducing one additional state is considered. This simple recomputation scheme guarantees high coverage of the FUs faults; moreover, low error detection latency is expected as all FUs are checked before the new output production.

The proposed CED technique deals with behavioral RT level models and is implemented through a set of transformation rules that can automatically be applied to the considered behavioral model.

## 2. Experimental results

To estimate the effectiveness of the proposed CED technique we hold a set of experiments. For this purpose

we considered two data dominated benchmark circuits: ELLIPF (it implements an Elliptical Wave Filter) and DIFFEQ (it solves a differential equation).

The original and CED designs (manually implemented for the considered benchmarks) were synthesized by means of the Synopsys Design Analyzer tool. We measured that the area overhead caused by the proposed CED technique introduction consists 62.0% for the ELLIPF benchmark and 24.9% for the DIFFEQ benchmark. As we can see, the area overhead in our case is much lower than that caused by the duplication of the whole design.

For the purpose of the fault coverage (FC) evaluation, single stuck-at faults were considered. In order to measure the FC the proposed approach attains, we exploited the following experimental procedure:

1. A set  $V$  of input stimuli was randomly generated composed of 10,000 vectors.

2. The benchmark including CED logic was fault simulated (using the Synopsys *faultsim* tool) while feeding the set  $V$  to its inputs. The list of faults  $TF$  that modified the expected circuit outputs was recorded.

3. The benchmark was then fault simulated again. The list of faults  $DF$  that the proposed CED scheme detected was recorded and the FC with respect to  $TF$  was measured, called *circuit fault coverage*.

By a similar procedure we measured the *functional unit fault coverage*, where faults affecting FUs only were considered.

FC results we obtained for the considered benchmarks are reported in table 1.

Table 1. Stuck-at fault coverage figures

Benchmark	Faults in TF [#]	Circuit fault coverage [%]	Functional unit fault coverage [%]
ELLIPF	11,350	76.1	100.0
DIFFEQ	23,232	94.7	99.6

## 3. References

- [1] R. Karri, B. Iyer, "Introspection: A Register Transfer Level Technique for Concurrent Error Detection and Diagnosis in Data Dominated Designs", ACM Trans. On Design automation of Electronic Systems, Vol. 6, No. 4, October 2001, pp. 501 – 515.
- [2] K. Wu, R. Karri, "Algorithm Level Re-Computing – A Register Transfer Level Concurrent Error Detection Technique", proceedings of IEEE/ACM International Conference on Computer Aided Design, pp. 537 – 543, 2001.