Technology Scaling Trends and Accelerated Testing for Soft Errors in Commercial Silicon Devices

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The soft error rate (SER) of advanced CMOS devices is now higher than all other reliability mechanisms combined. While most hard failure mechanisms exhibit product failure rates on the order of 1-100 FIT, the soft error rate of a low-voltage embedded SRAM can easily be 1000 FIT/Mbit! In this talk we consider the soft error sensitivity trends of various memory and logic components as they are scaled to smaller dimensions, higher integration densities, and lower operating voltages. We also review the three radiation mechanisms responsible for soft errors in the terrestrial environment and discuss the methods for characterizing radiation sensitivity and methods for extrapolating product SER from accelerated tests - with a focus on the difficulties in using test chip SER data to derive actual product mean-time-to-failure from soft errors. We then focus on technology scaling trends for SER, showing that although DRAM bit SER has been reduced by about four to five times per generation, DRAM system failure rates remain unchanged because the amount of system memory has increased as fast as the reductions in DRAM bit SER. We also show that in the deep sub-micron regime, the SRAM single bit SER saturates as a function of technology scaling. This saturation is attributed to reductions in the rate of voltage scaling (in the most recent technologies) and increased charge sharing due to short-channel effects. As with the DRAM case, this saturation trend in the SRAM single-bit SER does NOT translate to saturation in the SRAM system SER because of the rapid growth in embedded SRAM size. To the contrary, systems based on SRAMs, once considered SER proof, exhibit increasing failure rates with technology scaling - SRAM SER has now become a dominant reliability concern for some key applications. We review techniques for reducing SER and conclude that error correction is the best means of mitigating memory soft errors, and that in high reliability systems that employ error correction on all embedded memory, the product failure rate is limited by the sequential logic SER.

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