Keynote
Advanced EDA Tools for High-Performance Design

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Abstract

This talk will focus on Cadence's vision for advanced EDA tools and technology for high-performance designs at sub-nanometer process nodes. There will be specific emphasis on design for manufacturability to maximize yield, "reliable" design techniques and supporting technologies, and tool support for new high performance and low power circuit design techniques.

Biography

Ted Vucurevich serves as a Cadence Senior Vice President, responsible for driving advanced technology development and directing Cadence Laboratories. In addition, he serves as an executive fellow.

Vucurevich leads the Strategic Technology Office (STO). The STO researches, plans, and promotes a world-class Cadence technology roadmap and vision to Cadence employees, customers, and analysts. As director of Cadence Laboratories, Vucurevich represents Cadence on various external boards and interfaces between research efforts and product development.

In his prior role as chief architect at Cadence, Vucurevich helped develop the strategies and technology initiatives in system-on-a-chip (SoC)-based design, DSM infrastructure, software interoperability, design methodology development, and Internet-based electronic system design.

Vucurevich joined Cadence in 1992 as director of the Analog Physical Design group. In 1994 he was promoted to work as an architect in the Viper Development group. He was later named chief architect and held that position for five years. Prior to Cadence, Vucurevich worked 14 years at Analog Devices where he held roles in product, design, and computer-aided design (CAD) engineering. He was a co-founder of the Linear Signal Processing Division, where he was responsible for the implementation of a complete mixed-signal ASIC CAD environment.

Vucurevich received his bachelor of science degree in electrical engineering from the University of Arizona.