

Panel Discussion

System LSI Implementation Fabrics for the Future (special panel discussion)

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Abstract for Panel Discussion

IC design methodology and practice are going through major changes. The ASIC industry is being squeezed by FPGAs on one end, and by standard Ics on the other. Most of the changes are fueled by sub-100 nm process technology. The mask costs are skyrocketing, and first time silicon success is way down due to complications with process parasitics, cross talk, high device leakage current and other issues. The state of the art CAD tools are unable to deal with the process related complications and the ever increasing design complexity fully automatically. More than ever before, the involvement of the designer in critical CAD related decisions has exceeded the capacity of what we may rightfully expect from any individual.

Structured ASICs (SASICs) are one response to these problems. SASICs aim to fill a void between FPGAs and traditional ASICs. SASICs reduce design risk and complexity at the expense of design performance and possibly total cost, if the production volume is very high. SASICs are dismissed by some pundits as a mere marketing gimmick. Others claim SASICs are the long awaited salvage of the otherwise doomed ASIC industry. Predictions of SASICs disappearing in a few years are common. However, it is equally common to hear predictions that SASICs will expand tremendously and will push ASICs into a small corner of very high performance and very high production volume.

SASICs are still very much being defined in terms of their boundaries and their application space. Some SASICs are very close to traditional ASICs. Other SASICs are quite different; they are perhaps closer to traditional gate arrays in their look and feel. A third group of SASICs provide a much closer link with FPGAs.

In the panel discussion we will explore the fluid boundaries among ASICs, SASICs, and FPGAs. We will also explore different flavors of SASICs. We will discuss CAD tools and design methodology for SASICs. Of course, as any good panel should do, we will speculate on the implications of all these changes and what the future may bring. We may even come up with a few bold (and controversial) predictions about the fate of SASICs and what they will mean to the IC industry and IC CAD industry five years from now.