

# From IP to Platforms

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## Abstract

By 2010 over 95 percent of what is designed into Systems-on-a-Chip (SoC) will be IP (Intellectual Property). To effectively design these SoCs of the future, designers will need to make a conceptual shift from the current notion of “integrating IP into a design” to “integrating designs into IP platforms.” Assembling a platform consists of connecting IP blocks such as processor cores, memory block, peripherals, etc. using some interconnect fabric such as busses or a network-on-a-chip. The platform is further customized by specific logic and software. This presentation discusses the migration from IP to IP platforms, the key properties of IP that enable their effective assembly into platforms, and their use in design an verification.

## Biography

Dr. Raul Camposano joined Synopsys in January, 1994 and currently serves as Chief Technology Officer, Senior Vice President. He previously served as the General Manager of all Synopsys Design Tools Business Units and was also Vice President of Engineering. Prior to joining Synopsys, Dr. Camposano directed the German National Research Center for Computer Science Design Technology Center and was a Professor of Computer Science at the University of Paderborn, Germany. Between 1986 and 1991, Dr. Camposano led the project on high-level synthesis at the IBM T.J. Watson Research Center. Active in the EDA professional community, he also serves on various technical program committees and editorial boards worldwide and has published over 70 articles and three books on electronic design automation. He was elected IEEE fellow in 1999. Dr. Camposano holds a B.S. and an M.S. in E.E. from the University of Chile, and a Ph.D. in computer science from the University of Karlsruhe.