

ASICs, Processors, and Configurable Computing

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It is often suggested that configurable computing represents a new computational middle ground that fills the existing void between conventional microprocessors and ASICs. This point of view is based upon the observation that FPGAs share some similarities with both processors and ASICs. FPGAs are seen as similar to processors because they are customized in the field by the end-user by downloading configuration data into the device. They can also be seen as similar to ASICs because they can implement high-performance, application-specific circuits. It is hoped that if configurable computing can be shown to be similar to conventional processors, it will be possible to borrow microprocessor architecture and compilation techniques for use in the configurable-computing community.

However, configurable computing, as defined by current FPGA technology, does not fill the void between ASICs and processors. FPGAs hold much more in common with ASICs than they do processors. Indeed, if the spectrum of computing approaches were to be viewed as a family, ASICs and configurable computing would be siblings and processors would be distant relatives, at best. The distant relationship between FPGAs and processors can be seen best by studying the organization of *successful* FPGA applications, i.e., those applications that achieve at least order-of-magnitude performance gains over other processor-based approaches. A quick review of these applications shows that they are highly concurrent, deeply pipelined and achieve performance gains primarily by exploiting massive amounts of data-level parallelism -- typically 100-1000 times that of a general-purpose microprocessor. Contrast this with typical microprocessor applications that are described using sequential languages, implemented

as sequential instructions, and executed on machines optimized for sequential execution.

The relationships between configurable computing, ASICs, and microprocessors has several important implications. First, sequential programming languages and related compilation approaches are not likely to be a good match for highly parallel configurable-computing applications. While it may be possible to achieve moderate speedup, significant speedup will only be achieved by directly exploiting massive amounts of parallelism. This is currently done using low-level circuit design tools. Second, the architectural organization (both at the device and system level) will be much more distributed than is commonly found in existing computer systems. For example, whereas typical computing systems consist of large global memories, configurable-computing platforms will be much better served by many, smaller distributed memories. Finally, because of the fundamental mismatch between the datapaths in processors and configurable-computing systems, hybrid systems of microprocessors and FPGAs are best coupled in flexibly so that the best features of each device can be fully exploited.