

Combining General-Purpose and Multimedia in One Package: Challenges and Opportunities

Task Force Introduction

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Applications in graphics, video compression, image and audio signal processing have dictated a design philosophy for multimedia processors (MMPs) that is significantly different from general-purpose processors (GPPs). However, over the course of the last 18 months, the major processor vendors have extended their instruction sets to include many MMP features. For example, Sun has added the VIS instruction set extension into the Ultrasparc, HP has added the MAX-2 extension to the PA-RISC 2.0 architecture, and Intel has extended the x86 architecture with its MMX instruction set. At the same time, several other companies have been working on combined MMP/GPPs, including MicroUnity, Philips TriMedia, and Samsung.

The fusion of MMP and GPP raises some interesting questions, including:

- *Will multimedia extensions succeed in supplanting special-purpose hardware, or will they instead occupy a lower-performance niche?* Special-purpose MMPs have been the industry leaders for some time. They offer performance advantage for a modest cost. Although combined MMP/GPPs have a cost advantage (e.g., one package instead of two), they may not deliver equal performance due to, for example, memory bandwidth limitations. This leads to an additional question:
- *Is it possible to offer the highest MMP performance in the same package with the highest GPP performance?* The requirements of the two workloads are significantly different. Are the two workloads compatible, or will their requirements interfere?
- *Are new MMP designs sacrificing too much for GPP features, especially in sub-thousand dollar systems?* For new MMPs that are adding GPP features to existing designs, the overall cost of the part may be closer to GPP costs. For

portable/wireless systems, such costs may not be acceptable.

- *Is what we are seeing a fundamental shift in user workloads?* Computing workloads are more interactive and sensory than any time in the past. Are the additions to GPPs actually one step in the renewed evolution of our processor instruction set architectures? If so, should new designs emphasize multimedia over general purpose features?
- *Given the current instruction set extensions what additional extensions should be included, and at what additional cost?* The current extensions emphasize packed operations/minivectors. Is this style of operation sufficient? Or are other extensions needed? Are the new semantics sufficient to synthesize all the required MMP operations without undue impact on performance?
- *Are there added side benefits of multimedia extensions for GPP workloads?* If these operations have been implemented for one class of new workloads, are they going to be useful for integer code, for example? What extra ISA semantics would be helpful to facilitate this kind of usage?
- *What compiler support needs to be developed for the new, hybrid MMP/GPP processors?* It has long been the tradition in MMP to hand code algorithms in assembly. This tradition has been left behind for GPPs. Compiler techniques that can effectively exploit the new features will grow out of techniques for ILP processors and SIMD multiprocessors. But the engineering of the compiler must undergo a significant change to be able to handle such features as more than one value in a register, or automatic detection and usage of bit-reconfigurable, parallel ALUs.