

A Pipelined SoPC Architecture for 2.5 Gbps Network Processing

Ciaran Toal, Sakir Sezer, Xing Yu
School of Electrical and Electronic Engineering
Queen's University Belfast
Ashby Building, Stranmillis Road
Belfast, BT9 5AH, N. Ireland, U.K.
Ciaran.Toal@ee.qub.ac.uk

Abstract

This paper presents the architecture and implementation of a 2.5 Gbps Programmable Point-to-Point-Protocol Processor (P^5) on a Virtex II FPGA. A 32-bit wide pipelined processor circuit is implemented for layer 2 frame processing and a Leon processor core is embedded for higher layer PPP control protocol processing. An AMBA bus interface is used to interlink the Leon processor to the hardware frame processing unit and presents a standard interface allowing easy retargeting to other processor platforms. Complex memory control is implemented to enable the microprocessor to handle the extreme data rate. The high-level system breakdown is described and Virtex II synthesis results presented.

1. Introduction

The rapid growth in communication technologies and integrated services has brought about a need for scaleable and configurable networks. This need is accentuated by the convergence of network bandwidth and the processing limitations of off-the-shelf data products. In addition, with the merging of existing data communication systems and emerging services, there is an exigency to refine the support of Quality of Service (QoS) for new network equipment. It is clear, therefore, that to sustain this progression a network infrastructure that can adapt rapidly to keep pace with the needs of bandwidth and service diversity is required. As a consequence, programmability represents an essential component of next generation system architectures

Amid these developments, new direction in programmable and active networks is evolving. Network elements and systems, such as switches, routers, and multiplexers, can be reprogrammed with different signalling protocols and management agents by network operators, their customers and third parties. The need for programmability within the network layer has also been addressed with the development of a number of Network Processors by silicon vendors such as Intel, AMCC, Agere, IBM, PMC Sierra etc.

This paper presents the implementation of an architecture for layer 2 point-to-point protocol processing using Xilinx Virtex II FPGA technology with an open-source embedded soft microprocessor core.

Programmability is facilitated by using programmable logic and embedded software on a System on a Programmable Chip (SoPC) architecture.

2. The Point-to-Point Protocol

The Point-to-Point Protocol (PPP) [1], [2] provides a method for transmitting datagrams over point-to-point links and is the most efficient layer 2 protocol for encapsulating IP datagrams. PPP is a full-duplex simultaneous bi-directional link that is assumed to deliver datagrams in order. It provides a common solution for the easy connection of a wide variety of hosts, bridges and routers. Key applications include ADSL, dialup modems, encapsulated Ethernet, Virtual Local Area Networks (VLAN) and WANs.

The PPP performs three control functions. It provides an error-detecting framing method for encapsulating data over physical layer point-to-point links. It contains a Link Control Protocol (LCP) which establishes and tests the link, negotiates configurations and finally brings down the link when it is no longer needed. The PPP negotiates network-layer options independently from the network layer protocol by providing an individual Network Control Protocol (NCP) for each network layer supported.

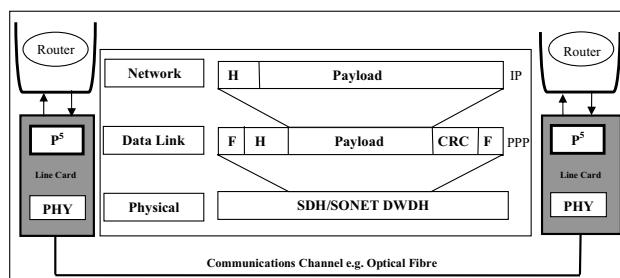


Figure 1 – P^5 System Embedded in Telecommunications Network

Figure 1 illustrates the physical location of the P^5 within a modern telecommunication system. The P^5 carries out data link functions and operates between a PHY chipset which establishes the physical connection between peers and a router which performs higher layer protocol functions e.g. IP routing.

3. SoPC System Architecture

The P^5 SoPC architecture is composed of three main units, a protocol data path unit, a protocol control path unit and an embedded microcontroller unit with an AMBA (Advanced Microprocessor Bus Architecture) bus interface [3]. Figure 2 illustrates this architecture showing the hardware/software partition and the hardware separation of the protocol control and the protocol data

paths. The soft-core Leon [4] processor is used for the control protocol functions.

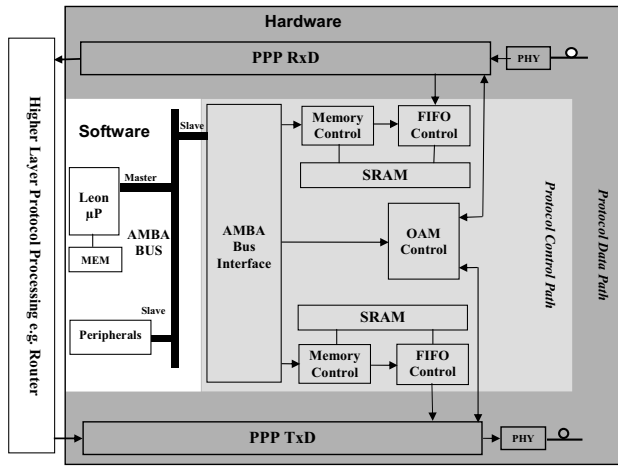


Figure 2 – P⁵ SoPC Architecture

The P⁵ protocol data path is a 32-bit wide circuit operating at a speed of 78.125 Mhz offering a data transfer rate of 2.5 Gbps. In order to achieve this performance, the P⁵ is sub-divided into two independent, parallel and highly pipelined circuits, one for transmitting data and the other for receiving data. The transmitter formats and packetises datagrams before transmitting over a physical link, while the receiver unpacketises and extracts the encapsulated datagrams from the received packets. A protocol filter at the receiver unit examines the protocol field of the received PPP frames and separates control protocols and user data protocols.

The P⁵ protocol control path handles the interaction between the Leon processor and the layer 2 protocol data path. It is composed of an Operation Administration and Maintenance (OAM) unit, a transmitter FIFO and a receiver FIFO for temporary storage of control protocols, a memory controller and an AMBA bus slave interface.

The protocol OAM unit provides an efficient interface for control and status information to be exchanged between the software controlled Leon microprocessor and the PPP transmitter and receiver units.

Two SRAM banks of 16 Kbytes (8 Block SelectRAMs) each, specifically for storing control protocol datagrams are included, one for the transmitter and one for the receiver. Two FIFO control units interface the P⁵ to the SRAM banks, and two memory control units interface the Leon processor to the SRAM banks. The complete layer 2 function is carried out by the PPP hardware leaving most of the higher layer control protocol functions to be carried out by the Leon processor.

The Leon microprocessor is interfaced to the P⁵ via an AMBA bus. Implementing the AMBA bus slave interface to the P⁵ in hardware allows that any hard or soft-

core microprocessor could easily replace the Leon soft-core by interfacing to the AMBA bus master.

4. Synthesis and Circuit Study

The P⁵ was synthesised and targeted to a Xilinx XC2V2000-6 device using Synplicity and Xilinx Foundation tools. The post-layout synthesis results are included in Table 1.

The Leon processor can only operate at approximately 46.6% of the speed at which the PPP receiver and transmitter units will be required to operate at. Two separate clock sources are incorporated to overcome this speed limitation. The Leon will be clocked at 25 Mhz while the speed critical transmitter and receiver units will be controlled by a 78.175 Mhz clock source.

	Logic Resources			Speed (MHz)
	Slices	LUTs	SelectRAM	
PPP Transmitter and Receiver	1144	2157	0	78.66
OAM, Memory Logic, AMBA Interface	631	1126	16	81.5
Leon Processor	2845	4784	6	36.68
Total	4620 (43%)	8067 (37.5%)	22 (39.3%)	

Table 1 – Post Layout Synthesis Results for Xilinx XC2V2000-6 (Foundation)

Altogether 4620 slices of logic resources are required from 10,752 available on the XC2V2000. This is approximately 43% of what are available allowing extensive routing resources for place and route tools. The above synthesis however does not include Leon program memory which is allocated in external SRAM banks.

5. References

- [1] W. Simpson, "PPP over SONET/SDH", Internet Engineering Task Force, RFC1619, May 1994
- [2] W. Simpson, "The Point-to-Point Protocol", Internet Engineering Task Force, RFC1661, July 1994.
- [3] R. Weiss, "Advanced Microprocessor Bus Architecture (AMBA) bus system", Electronic Design, vol.49, no.5, 5 March 2001, pp.114-15. Publisher: Penton Media, USA
- [4] J. Gaisler, "A portable fault-tolerant microprocessor based on the SPARC V8 architecture", DASIA 99. Data Systems in Aerospace. Lisbon, Portugal. 17-21 May 1999.