

Synthesis for Industrial-Scale Analog Intellectual Property

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Abstract

Analog synthesis tools have traditionally traded quality for speed, substituting simplified circuit evaluation methods for full simulation to accelerate the numerical search for solution candidates. I will argue that this is no longer an acceptable tradeoff: for a synthesis strategy to have practical impact, it must use a simulator-based evaluation engine identical to that used to validate ordinary manual designs. Put more bluntly: to trust a synthesis result, you must first trust the methods used during synthesis to measure that your circuit really works. Prior analog synthesis work fails here.

Simulation-based synthesis, however, poses significant challenges. Commercial simulators are not designed to be invoked 50,000 times in any optimizer loop. I will describe a synthesis methodology and new global search algorithms that are efficient enough to allow full circuit simulation of each solution candidate, yet robust enough to find good solutions for difficult circuits.

Finally, to counter the criticism that analog synthesis can never scale to cope with the complexity of industrial designs, I will show how the use of appropriate macromodeling techniques allows us to attack complex analog blocks. I will describe how we resynthesized from scratch, in several different styles, the equalizer/filter block from the frontend of Texas Instrument's production ADSL CODEC [Hester et al, ISSCC99] and verified that our designs matched TI's original specifications. This is the largest manual-vs-synthetic controlled experiment ever undertaken with a state-of-the-art design. Coupled with emerging commercial tools for analog physical synthesis, I will argue that we are finally able to consider synthesis of nontrivial blocks of analog IP.