

Reconfigurable Computing at Xilinx

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In the last decade and a half, Field Programmable Gate Arrays (FPGAs) have grown from simple devices with a few hundred programmable logic gates to densities beyond one million gates. This growth in density has led to an ever-expanding area of application for these devices. From their early use as simple interface or “glue” logic, FPGAs have moved on to become popular platforms for implementing system bus interfaces, including industry standards such as PCI. As device density has surpassed one million gates, FPGA co-processing in data-intensive applications such as Digital Signal Processing (DSP) and networking has become commonplace. The recent announcement of the Virtex II FPGA + CPU device from Xilinx, as well as similar announcements from other vendors, indicate that the trend toward single chip FPGA + CPU processing will continue. And with ten million gate devices under development, it is expected that more system functionality, including more general-purpose processing, will continue to migrate into the FPGA.

While much of this type of coprocessing can also be accomplished with fixed Application Specific Integrated Circuit (ASIC) hardware, the ability to reprogram FPGA devices, even in system, opens up new opportunities for system design. Reconfigurable logic provides new methods for increasing performance, decreasing power consumption and increasing system functionality. Along with these new benefits come challenges, particularly in the area of software design tools. Tools such as Xilinx’s JBits point the way toward providing a single unified environment for programming CPUs, configuring and reconfiguring hardware resources and providing integrated debug support for the single chip reconfigurable systems of the future.