Behavioural Modelling of Operational Amplifier Faults using VHDL-AMS

Peter R. Wilson, Yavuz Kiliç [†], J. Neil Ross, Mark Zwolinski, Andrew D. Brown

University of Southampton,
Department of Electronics and Computer Science,
Southampton, United Kingdom

[†]Philips Semiconductors,
Southampton,
United Kingdom

Abstract

The use of behavioural modelling for operational amplifiers has been well known for many years and previous work has included modelling of specific fault conditions using a macro-model. In this paper, the models are implemented in a more abstract form using an Analogue Hardware Description Language (AHDL), VHDL-AMS, taking advantage of the ability to control the behaviour of the model using high-level fault condition states. The implementation method allows a range of fault conditions to be integrated without switching to a completely new model. The various transistor faults are categorised, and used to characterise the behaviour of the HDL models. Simulations compare the accuracy and speed of the transistor and behavioural level models under a set of representative fault conditions.

1 Introduction

It is becoming increasingly necessary to use mixed signal simulation to understand the behaviour of circuits under fault conditions. The two main types of approach are specification based [1] and fault model based [2-6]. These approaches require the use of behavioural modelling to reduce the simulation times required [7]. Proprietary languages (MAST [8]) or standard languages such as IEEE 1076.1 (VHDL-AMS) [9] may be used to model elements such as operational amplifiers, including the Boyle macro-model [10]. This paper deals with the equation-based approach to implement fault behavioural model [12] using VHDL-AMS.

2 Modelling and Simulation

To demonstrate the concepts used in this paper, the IEEE Mixed-Signal Benchmark circuits have been used [11], modeled using transistor level circuits, and equation based fault models. The models defined in [12] was implemented as a behavioural model using VHDL-AMS. The models were tested and compared well with transistor level simulations. A comparison was also made between the simulation times as shown in table 1.

3 Conclusions

In this paper, a method of implementing fault behavioural models for operational amplifiers has been presented. Previous work has been extended to cover both the open and closed loop configurations allowing greater flexibility in the application of the fault models in the general case. Results show a good correlation between transistor and behavioural models at all stages, with a corresponding improvement in simulation times.

Circuit configuration	Device (s)	Behavioural (s)
Inverting Fault Free	1.88	0.1
Inverting Fault I	1.78	0.1
Inverting Fault II	1.81	0.1
Inverting Fault III	1.89	0.15
Non-Inverting Fault Free	1.89	0.1
Non-Inverting Fault IV	1.89	0.45
Biquad Filter (a)	11.1	2.35
Biquad Filter (b)	93.2	2.49

Table 1 : Comparison of Simulation Times

4 References

[1] Voorakaranam and Chatterjee, "Hierarchical specification driven analogue fault modeling for efficient fault simulation and diagnosis", *IEEE International Test Conference*, 1997, pp903-912

[2] Perkins, Zwolinski, Chalk & Wilkins, "Fault Modeling and Simulation using VHDL-AMS", *Analogue Integrated Circuits and Signal Processing*, 16, 1998, pp141-155

[3] Pan & Cheng, "Fault Macromodeling for Analogue/Mixed Signal Circuits", *IEEE International Test Conference*, 1997

[4] Milor & Visvanathan, "Detection of catastrophic faults in analogue integrated circuits", *IEEE Trans. on Computer Aided Design (CAD)*, 8, 2, 1989, pp114-130

[5] Sounder & Stenbakken, "A comprehensive approach for modeling and testing analogue and mixed signal devices", *Proc. of International Test Conference*, 1990, pp169-176

[6] Nagi, Chatterjee, Balivida, & Abraham, "Fault based automatic test generator for linear analogue circuits", *Proc. of International Conference on CAD*, 1993, pp88-91

[7] Kilic & Zwolinski, "Behavioural/Macro modelling to speed up analogue fault simulation", ELECO 2001

[8] MAST Reference Manual, Avant! Corporation , USA

[9] IEEE Standard 1076.1 (VHDL-AMS)

[10] Boyle, Pederson, Cohn & Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid State Circuits*, 1974, pp353-363

[11] Chang, Lee, Chen, & SU, "A Behaviour Level Fault Model for the Closed-Loop Operational Amplifier", *Journal of Information Science and Engineering*, 2000, 16, pp751-766

[12] Wilson, Kilic, Ross, Zwolinski & Brown, “Behavioural Modeling of Operational amplfier Faults using analogue Hardware Description Languages (HDLs)”, BMAS 2001

Proceedings of the 2002 Design, Automation and Test in Europe Conference and Exhibition (DATE’02)
1530-1591/02 $17.00 © 2002 **IEEE**