Mappability Estimation of Architecture and Algorithm

Juha-Pekka Soininen, Jari Kreku & Yang Qu
VTT Electronics, Kaitoväylä 1, FIN-90570, Oulu, Finland
e-mail: juha-pekka.soininen@vtt.fi

Abstract

Method for the selection of processor core and algorithm combinations for system on chip designs is presented. The method uses a mappability concept that is an addition to performance and cost metrics used in codesign. The mappability estimation is based on the analysis of the correlations of algorithm and core characteristics. The method is demonstrated with an analysis tool and the experimental results with DSP cores and algorithms are similar to expectations.

1. Introduction

The design of integrated multicomputer system will extend the problems faced with current system-on-chip design with system level and computer architecture design problems. Performance design with analyses, simulations and measurements have been used in computer architecture design. The hardware complexity and software performance estimation based cost functions have been used in the codesign.

In the presented mappability estimation method the analysis is based on comparing the characteristics of algorithms and processor cores instead of mimicking the execution. The result describes the potential quality of the system and it can be used in comparison of cores or algorithms during design space exploration.

2. Architecture-algorithm mappability

The figure of merit proposed for architecture-algorithm pair is mappability. It is optimal when the core's hardware architecture does not constrain the execution and it does not have any unused capacity. In ideal case all the hardware in core are participating into execution of code all the time, but additional gates could not be used because of the nature of code.

The proposed method extracts essential characteristics of the core and algorithm and analyses how much correlation exists between algorithm's data dependencies and control flow structure and core properties.

In the overall mappability the **functional unit correlation** M_{FU} expresses how effectively and extensively core's instruction set has been used for the given algorithm. **Memory interface correlation** M_{MI} expresses how effectively registers and buses can be used. **Execution architecture correlation** M_{EA} expresses whether the algorithm execution can benefit from parallelism and pipelining provided by the core. The values are scaled between [0,1], where one is the optimal mappability.

The presented analysis method is implemented using SUIF2 compiler and a correlator-tool written with C++. The method has been tested using ADSP-2181 and TMS320C6201 DSP core models. *Search* algorithm searches for a text string from data stream. *Table* calculates the sum of elements of a one-dimensional table. *Matrix* is multiplication of two 4 x 4 matrices. *FIR* filter and *WLAN* synchronisation are real DSP algorithms.

Table 1: Correlation results.

		M_{EA}	M_{MI}	M_{FU}	M_{Total}
Texas C6201	Search	0,56	0,42	0,08	0,35
	Table	0,71	0,62	0,38	0,56
	Matrix	0,36	0,28	0,14	0,26
	FIR	0,62	0,36	0,21	0,40
	WLAN	0,64	0,47	0,06	0,38
ADSP 2181	Search	0,60	0,96	0,51	0,68
	Table	0,32	0,38	0,40	0,36
	Matrix	0,16	0,08	0,01	0,09
	FIR	0,47	0,50	0,50	0,49
	WLAN	0,41	0,62	0,36	0,45

Simple algorithms clearly favour ADSP-2181 whereas TMS320C6201 has better mappability values with algorithms that have more parallelism. In all algorithm cases the results are equal to expectations. The estimation does not take into account the absolute performance, which is naturally better for TMS320C6201.

3. Conclusions

The paper presents a method for estimation of algorithm-architecture mappability, which can be used at the selection of processor cores in the design of multiprocessor system on chips or in identifying required core characteristics. The method is demonstrated with prototype tool. The calculated estimates correlate quite accurately with the expected behaviour of real architecture-algorithm pairs.

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