On–Chip Inductance Models: 3D or not 3D?†

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Abstract

Full 3D lumped partial inductance models usually contain a tremendous amount of forward coupling terms. To reduce the complexity of simulation and analysis, a simplified model that excludes the forward coupling terms is often adopted in practice [3][4]. This paper addresses the question whether ignoring forward couplings is always an acceptable choice or if full 3D models are necessary in certain cases. We show that the significance of the forward coupling inductance depends on various aspects of the design.

1. Introduction

Accurate PEEC models for on-chip interconnects can be obtained via field-solution based three-dimensional capacitance and inductance extraction programs. However, unlike coupling for capacitance, inductance coupling between conductors decreases very slowly with distance. Therefore the full RCL PEEC models often have to include an order of magnitude more coupling elements than the RC models, thereby creating a daunting task for the subsequent simulation and optimization steps.

Note that the dominant portion of coupling inductance terms are due to *forward coupling* between non-parallel conductor segments, and in practice these terms are often removed for modeling simplicity and matrix sparsity[3][4]. With the forward coupling terms discarded, the coupling inductance terms only exist in the direction orthogonal to the direction of current, therefore we refer to this as a two-dimensional (2D) partial inductance model. (Note that the partial inductance of a uniform long wire grows superlinearly, therefore defining the 2D partial inductance model based on infinitely long wires will result in infinite unit length inductance values.)

Although it has been shown experimentally that for specific designs (shielded clock-trees) these simplified inductance models are able to produce results with satisfying accuracy[3], to date, no analysis has been performed on their general applicability.

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In this work we first analyze the magnitude of the forward coupling inductance between segments of long parallel wires under different current return situations. Analytical inductance formulas ([1][2]) are applied to derive the relative magnitude of forward coupling and self inductance terms. It is shown that the impact of the forward coupling terms largely depend on the actual current return paths. We conclude that due to the "dipole" effect, the forward coupling inductance is effectively negligible in the cases when the interconnect design causes all of the current to return from nearby parallel conductors -- e.g., extensively shielded busses and clock-trees. Error analysis of the 2D model vs. the full 3D model are performed analytically and demonstrated with coplanar examples (Fig. 1). The applicability and the limitation of the 2D linear model is addressed in the scenario of real on-chip interconnects.

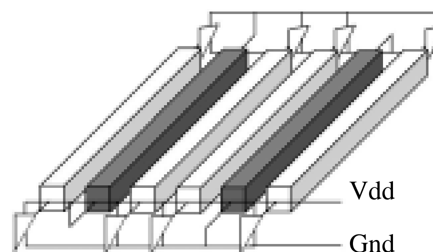

Fig. 1: A parallel coplanar structure

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