On Nanoscale Integration and Gigascale Complexity in the Post .Com World

Hugo De Man, Professor, KU Leuven, Senior Research Fellow, IMEC, BE

While process technologists are obsessed to follow Moore's curve down to nanoscale dimensions, design technologists are confronted with gigascale complexity. On the other hand, post-PC and post dotcom products require zero cost, zero energy yet software programmable novel system architectures to be sold in huge volumes and to be designed in exponentially decreasing time. How do we cope with these novel silicon architectures? What challenges in research does this create? How to create the necessary tools and skills and how to organize research and education in a world driven by shareholders value? Can you spare half an hour to reflect on these challenges to the design community?

Global Responsibilities in SoC Design

Taylor Scanlon, President & CEO, Virtual Silicon Technology, US

The technical complexities of advanced SoC design are compounded by changes in the economic structure of the worldwide semiconductor industry. A look at some of the organizational and personal responsibilities that will be required to meet the challenges of SoC design in the Future

Proceedings of the 2002 Design, Automation and Test in Europe Conference and Exhibition (DATE'02)
1530-1591/02 $17.00 © 2002 **IEEE**

IEEE COMPUTER SOCIETY