

# Test Pattern Length Required to Reach the Desired Fault Coverage

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An essential point in VLSI (very large scale integration) testing is to build a testing strategy that can produce the best solution for the selection of a testing method which takes into account such factors as quality, cost (chip area, yield, testing cost, etc.), performances, power dissipation and time for the development project, as well as for the determination of the role of the tester. For this purpose, it is important to know the relationship between the fault coverage  $F$  and the pattern length  $L$  in order to obtain the testing cost and the defect level that will serve as the quality indicator. Some studies have already disclosed the relationship between the fault coverage of pseudo random-number generation patterns and the pattern length in BIST. In these studies, the discussion uses a delta function for the distribution function of the detected faults. However we discuss conventional testing methods, with the exception of BIST, as well as the relationship between the fault coverage and the pattern length based on the assumption that the distribution function of the detected faults is a gamma distribution.

Under this assumption, the probability of fault detection becomes the negative binominal distribution from the binominal distribution and is approximated as the negative hypergeometric distribution. Since, based on the definition of the negative hypergeometrical distribution and on the definition of the negative binominal distribution, the clustering parameter  $k$  plus the number of detected faults  $M$  represents the number of trials, the subject of our discussion therefore indicates the length of the execution test pattern. Then we assume that pattern compression and expansion are in proportion to the total fault number  $N$  and to the detected fault number. And we assume that pattern compression and expansion are in inverse proportion to the number of terminals  $P$ . As we can assume that the total

number of detected faults is given by the greatest value of detected faults, we assume that the total number of faults detected by the test pattern is the mean value plus 3 sigmas of the negative binominal distribution. Consequently we can get the execution test pattern length.

Here, with  $C$  as the pattern compression coefficient, the execution test pattern length  $L$  is given by the following equation.

$$\begin{aligned} L &= CN/P M(k+M) \\ &= CN/P [kF/(1-F)+3(kF)^{1/2}/(1-F)] \\ &\quad [k+kF/(1-F)+3(kF)^{1/2}/(1-F)] \end{aligned}$$

And the processing time of an ATPG (Automatic Test Pattern Generator) varies greatly according to the CPU speed and algorithm. Assuming here that the time required to generate the test pattern  $T_{ATPG}$  is in proportion to the time  $T_1$  for generating the test pattern required to detect a given number of faults, and in proportion to the detected fault number  $M$ ,  $T_{ATPG}$  can be obtained by the following equation.

$$\begin{aligned} T_{ATPG} &= MT_1 \\ &= [kF/(1-F)+3(kF)^{1/2}/(1-F)]T_1 \end{aligned}$$

In this study, we defined the relationship between the fault coverage and the execution test pattern and found the validity of our theory by proving that this relationship agrees with the actual values using single stuck-at fault coverage as the fault coverage. We believe that our theory will enable the prediction of the execution test pattern length (=testing time) and ATPG processing time required to reach the desired fault coverage at an early stage of the design of the devices and to provide early solutions for problems arising during test development.