

# Outstanding Challenges in Testing Nanotechnology Based Integrated Circuits

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## Summary

Before we list the *outstanding challenges*, meaning *what remains to be done*, we need to ask the following questions: 1) What has changed to require this rethinking? 2) What solutions are still applicable in today's environment? and 3) What is likely to happen in the future?

The answer to the first and the third questions is that the technology is changing (shrinking dimensions) at a very fast rate, without any signs of slowing down. But we also know that this exponential growth rate is not sustainable. What I mean is that the time when slowdown is likely to occur is highly unpredictable. In spite of this uncertainty, we still can use the general growth trends from the past to identify the characteristics of the new problems and describe desirable characteristics of the solutions.

It is certain that the *complexity* of devices has grown. This multidimensional word encompasses area (large ICs and resulting yield and reliability issues), large number of components on a single IC (mixed signal designs, IP cores, and SoC issues), and performance (clock frequency issues) requirements, all in addition to meeting the power demands (peak and average) of the designs. There is no single agreed upon cost metric that satisfies all these requirements. Thus, in general, there are tradeoffs and the solutions that have been proposed target only some aspects. None the less, areas of research that are starting to dominate, and correctly so, are the following.

Traditionally, we have been focusing on the performance of ATPG systems and fault simulators targeting stuck-at faults. We will still have to continue on this path but we will need to manage even larger designs with the additional condition that the impatient designers and the sales managers would like to see it done even faster. This includes handling of *new faults*, such as capacitive and inductive crosstalks, and the test community will need to develop faster simulation technology than the one developed and used by the design community. However, this research will impact only the fixed cost component, the cost that is amortized over all the devices, of testing.

Power delivery to the devices during the normal as well as during the test, is largely a domain of the design research. Test requirement in this direction is some what moderate and the focus of research in this direction will largely be in scheduling of tests. However, I believe that this component of test will only have a limited impact on the fixed as well as the variable cost of test.

Finally, the variable cost, the cost of testing each device, will be dominated by the *test application time*, given by the equation:

$$\text{Test Application Time} \approx (\text{Number of Gates})^k$$

where  $k > 1$  and is between 1.1 and 1.3. Thus, this cost is growing at a rate faster than the design complexity. We believe that the relative growth is even higher if we allow for testing of faults from the more esoteric fault models for the nanotechnologies. Hence, we need to develop novel solutions to the test application problem. This may mean re-looking at the most often used DFT and BIST methods. Also, we will need to develop new and superior test generators and fault simulators that can handle faults from the new fault models and possibly deal with multiple faults.

The presentation will raise questions in all three dominant domains in the area of testing: traditional issues, power issues, and test application time issues.