

# A Low-Power LFSR Architecture

Tsung-Chu Huang

Kuen-Jong Lee

Dept. of E.E., Nat'l Cheng Kung Univ., Taiwan

LFSR's are widely used in the BIST environment. In [1] a multiphase technique is proposed to reduce the data transitions (DTs) in both the LFSR and the circuit under test. However, its multiphase clock generator is implemented by a conventional Johnson counter with a complex control logic, which requires considerable area overhead and power dissipation. Also the employed dynamic demultiplexers may consume much power. In this paper, we develop a low-power multiphase clock generator, employ static demultiplexers and propose a hybrid design to reduce the power. The power model is based on the *weighted transition count* (WTC) [2]. The internal gates of a latch consume 2 transitions per cycle when the data changes. The clock and data input capacitances of a latch are assumed the same as that of a regular gate. A double-latch FF thus consumes 5 transitions including the interconnection between latches when the data changes.

Our design can be described as follows. First, a conventional  $n$ -phase clock generator usually employs an  $\frac{n}{2}$ -FF Johnson counter. We propose to replace each FF with a latch as shown in Fig. 1, where correct  $n$ -phase clock signals can still be generated without the *data transparency* problem if the odd and even latches are in complemented (low- or high-level enabled) types and each enabled latch has the same data as its preceding latch. With this latch-based Johnson counter the WTC can be reduced from  $2n + 10$  to  $\frac{n}{2} + 17$  per cycle. Second, in a conventional  $k$ -phase shift register ( $k\Phi SR$ ) as shown in Fig. 2(a), the demultiplexer is implemented by joined transmission gates, which actually consume much power at joint *out*. We modify the output stage as Fig. 2(b) shows. During phase  $i$  only  $\Phi_i$  will be high and only the data  $D_{k-i}$  may change with a probability of  $\frac{1}{2}$ . The  $k\Phi SR$  consumes 2 and  $\frac{k}{2}$  transitions in the demultiplexer and the data input, respectively. The active FF thus consumes  $\frac{5}{2}$  transitions in average in its internal gates and 2 transitions at the clock input. Therefore, the  $k\Phi SR$  takes  $\frac{k}{2} + \frac{15}{2}$  transitions per cycle. Finally, single- and multi-phase clock schemes are combined in a hybrid LFSR design taking the advantage of sharing a  $k$ -phase clock generator by multiple  $k\Phi SR$ . Fig. 3 shows an example with  $c(x) = 1 + c_1x + c_2x^2 + \dots + c_{n-1}x^{n-1} + x^n$ , where contiguous coefficients  $c_{j+1}, c_{j+2}, \dots, c_{j+k-1}$  are zeros.

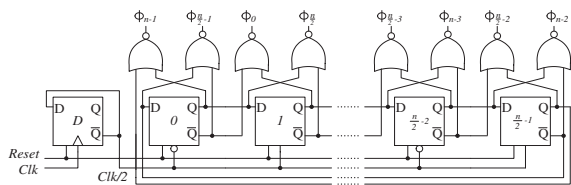


Figure 1: A  $n$ -phase multiphase clock generator.

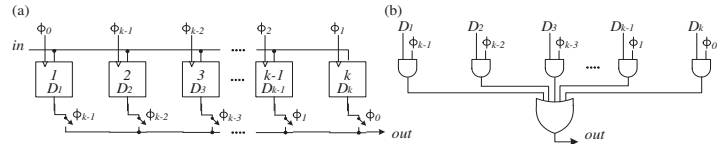


Figure 2: (a) A  $k\Phi SR$  and (b) its output bus.

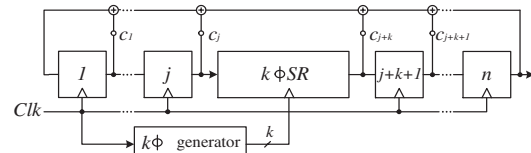


Figure 3: A hybrid LFSR.

A 2-tap LFSR with  $c(x) = x^n + x + 1$  with  $k = n - 1$  is used as an example to estimate the power reduction. The transition counts of the conventional design, the design in [1] and our architecture are compared in Columns *Conv.*, *Work[1]* and *Ours* of Table 1. Rows 1 and 2 show the transition counts of a multiphase SR and clock generator, respectively. The transition count per cycle due to the XOR gate is 1. From Rows 4-6, only the conventional and our designs use FF's in serial connections. As a result, the total transition count of a LFSR can be reduced from  $7n + 1$  of a conventional design or from  $3n + 16$  of the MFSR in [1] to  $n + 32.5$  in our design. When  $n > 27$ , our design can have more than 40% power reduction compared with previous work and 70% compared with the conventional LFSR.

Table 1: Transition counts of a 2-tap multiphase LFSR.

Item	<i>Conv.</i>	<i>Work[1]</i>	<i>Ours</i>
Multiphase SR	-	$n + 5$	$(k + 15)/2$
Multiphase Clk generator	-	$2n + 10$	$\frac{k}{2} + 17$
Inputs of 1 XOR gate	$2 \times \frac{1}{2}$	$2 \times \frac{1}{2}$	$2 \times \frac{1}{2}$
Clock tree to serial FF's	$4n$	-	$4 \times (n - k)$
DTs in serial FF's	$\frac{1}{2} \times 5 \times n$	-	$\frac{1}{2} \times 5 \times (n - k)$
Inputs of serial FF's	$\frac{1}{2} \times n$	-	$\frac{1}{2} \times (n - k)$
Total (when $k = n - 1$ )	$7n + 1$	$3n + 16$	$n + 32.5$

## References

- [1] M. Lowy. Parallel Implementation of LFSR for Low Power Applications. *IEEE Trans. on Circuit and System*, 43(6):458-466, Jun. 1996.
- [2] T.-C. Huang and K.-J. Lee. Reduction of Power Consumption in Scan-based Circuits during Test Application by an Input Control Technique. *IEEE Trans. on CAD of Circuits and Systems*, 20(7):911-917, Jul. 2001.