

Built-In Self-Test for State Faults Induced by Crosstalk in Sequential Circuits

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1. Introduction

With the moving into deep submicron (DSM) technology and GHz clock frequencies, signal integrity problems become important [1]. Signal integrity problems are induced by circuit noises such as crosstalk, power supply noise, substrate noise, etc. In this paper, we consider crosstalk in such noises and propose a new Built-In Self-Test method for faults induced by crosstalk, called crosstalk faults.

2. Built-In Self-Test for crosstalk faults

In this paper, we deal with the case that aggressor is a data line and victim is a clock line. And we assume that aggressor and victim corresponds to one-to-one. In addition, we handle the circuit that a clock buffer is inserted in the clock line of every FF. Hence, only one FF is affected by an additional clock as shown hatched FF in Fig. 1.

In the proposed BIST circuit, switches are inserted in inputs of state FFs as shown in Fig. 1. In the test mode, switches are opened to disconnect inputs of FFs and outputs of the combinational circuit. And LFSRs with the pre-determined number of stages are configured by using state FFs. These LFSRs have the same characteristic polynomial. If the total

number of FFs in the circuit is not a multiple of LFSR stages, a proper number of FFs are added to the circuit.

Primary inputs are connected to LFSRs to apply test vectors as shown in Fig. 1. Likewise the state FF, these LFSRs are configured with the pre-determined number of stages and have the same characteristic polynomial. But the characteristic polynomial of LFSRs connected to primary inputs is different from the characteristic polynomial of state FFs. Moreover, we configure the LFSRs by using the input block FFs of this chip in order to implement the BIST circuit with low area overhead.

Delay gates are inserted in outputs of LFSRs as shown in Fig. 1. In the test mode, outputs of LFSRs are connected through delay gates in order to avoid a setup violation. In the normal mode, delay gates are bypassed through the bypass line attached to delay gates shown as a dotted line in Fig. 1.

When a crosstalk pulse is generated on a clock line as an additional clock pulse, the FF changes its value if the input and the output of the FF have different values. Therefore the LFSR including the affected FF has different value with other LFSRs. As shown in Fig. 1, the bottom position of LFSR is connected to the comparator. The fault can be detected by comparing the value of this position for every clock.

3. Experimental results

Table 1 shows the experimental results for some ISCAS'89 benchmark circuits. In this paper, 100 and 150 stages of LFSRs are used. The number of applied vectors is 200000 in each experiment. The table shows that more than 99% coverage is obtained for almost circuits.

Reference

- [1] K. L. Sheppard, and V. Narayanan, "Noise in Deep Submicron Digital Design," Proc. of ACM/IEEE Design Automation Conference, pp. 524-531, 1996.

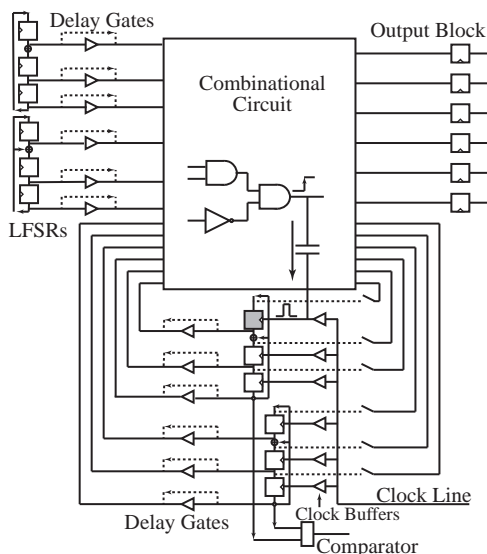


Figure 1 Diagram of BIST circuit

Table 1 Experimental results

Circuit	# of PI	# of FF	# of Fault	100 stages		150 stages	
				Cov. (%)	Area overhead (%)	Cov. (%)	Area overhead (%)
s13207	31	669	5772132	99.09	13.12	99.61	15.63
s15850	14	597	6182532	98.70	9.43	99.63	9.33
s35932	35	1728	30806784	99.78	15.47	99.86	15.30
s38417	28	1636	38997332	99.53	11.81	99.57	10.75
s38584	12	1452	29837148	99.55	11.47	99.19	11.34