

# High-Speed Interface Testing

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## 1.Problem of High-Speed Interface Macro Testing

Because the function of the chip is guaranteed, the high-speed function test is important. Moreover, it is an important issue in LSI test how cheaply to do this test. The high-speed function test in an internal logical circuit can be tested by using BIST methodology and the output clock of PLL with a low-speed and low-cost ATE. However, the high-speed function test to the Interface macro should do the interface at high speed between the Interface cell and the ATE. Therefore, a high-speed ATE is needed for this. This ATE is very expensive, and enlarges the test cost of the product which builds in this macro. It is a issue of the semiconductor vender who offers the product with High-Speed Interface to reduce the test-cost of this without lowering the quality of the product.

## 2.High-speed function test methodology of High-Speed Interface Macro

Our company developed the high-speed test methodology of loop back test technique for the issue mentioned above.

### (1)Circuit composition

Figure 1 shows the outline of this test methodology.

100 of Figures 1 is a receiver of a High-Speed Interface Macro (input). This is composed of LVDS/CML, CDR (Clock Data Recovery) and MUX(converter of parallel data to serial data). The CDR circuit is a circuit which selects the most suitable clock for the phase of the input data of the receiver from n clocks (The phase of each f/n shifts though each clock is this frequency) output from PLL. Because this

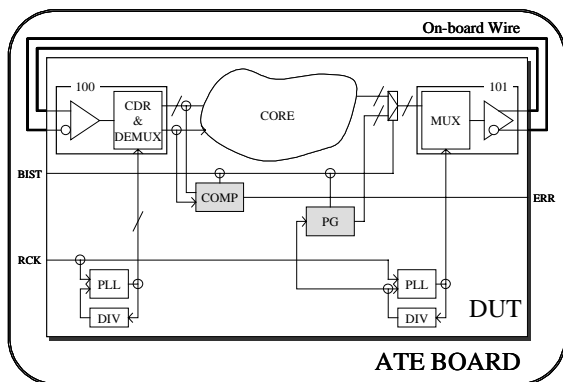


Figure 1 Overview

circuit is designed according to the function frequency of the macro, it does not operate accurately excluding the range of the frequency

101 is composed of LVDS/CML and Demux(converter of serial data to parallel data) by transmitter of a High-Speed Interface Macro (output). PG(data generator) is connected with the input of transmitter and COMP(comparator) is connected with the output of the receiver. The I/O terminals of transmitter and receiver are connected on the ATE board, and the BIST circuit which encloses High-Speed Interface Macros is composed on the board.

### (2)Test Function

The loop back test function is explained as follows.

- 1)The PG circuit generates parallel input data to transmitter.
- 2)The parallel data input to transmitter is converted into the serial data of the same frequency as the output clock frequency of PLL through the MUX circuit.
- 3)The high-speed data generated with the MUX is output to the ATE board through the LVDS/CDR of transmitter.
- 4)The output data of 3) is passed on to the input terminal of the receiver through wiring on the ATE board. There is no limitation of the terminal location of the receiver and transmitter when the loop-back test is done. Each signal line of Posi/Nega should be equal length. Moreover, this wiring should be length in the driver ability of LVDS/CML. This test methodology is called "loop back test" from the output of wiring on this ATE board from DUT and the input to same DUT.
- 5)The data input to the receiver is returned to the data of n bit of the frequency 1/n time through the CDR& Demux circuit. The data is input to the COMP circuit, and it is compared with the expected value data output from the PG circuit.
- 6)The test result of the record in the COMP circuit after the test is completed is confirmed, and Pass/Fail of high-speed function of the High-Speed Interface Macro is judged.

### (3)Result

The following results were achieved by this method.

- 1)An expensive high-speed ATE was not used, so the test cost was able to be reduced greatly though there it was necessary to make the ATE board only for a high-speed interface testing.
- 2)When the test did not work by the ATE skew of a high-speed ATE, we changed the input signal timing, so the test throughput was bad. We improved the test throughput by this method.
- 3)This method was not an indirect guarantee by a low-speed testing, so the test quality equaled with the result of using a high-speed ATE was able to be secured.
- 4)The super-high-speed interface(5Gbps, 10Gbps, ...) testing which was not able to be tested even with a high-speed ATE became possible.

## 3.Summary

One big problem to the high-speed interface macro development and the support for the high-speed network business which Fujitsu held was able to be solved by this loop back testing technique. In future, we want to advance the examination of the higher quality and the further efficiency improvement for the test cost reduction.