

An Application of Partial Scan Techniques to a High-End System LSI Design

Toshinobu Ono¹ Akira Kozawa² Takashi Kimura² Yoshihiro Konno¹ Koji Saga¹

¹NEC Corporation

²NEC Software Hokuriku, LTD.

1. Introduction

In large and high-speed LSI designs, the area and delay overhead of the design-for-test (DFT) circuit must be minimized while keeping sufficient testability. Partial scan is one of the techniques that can reduce the overhead of full scan. However, it is not simple to apply the partial scan method to large designs because of its long design turn-around-time (TAT) and pattern length.

This paper presents an application of the partial scan method to a real LSI design. Several techniques have been introduced in order to effectively apply the method to the large high-end system LSI.

2. Target Design

The following are the approximate statistics of the target LSI to which partial scan DFT has been applied.

Process: 0.18 μ m CMOS
Transistors: 60,000k (24,000k in logic part)
Flip-flops: 240k
Latches: 70k

3. Scan Structure

Since a hierarchical design methodology is used in designing the LSI, DFT and automatic test pattern generation (ATPG) are also done in a hierarchical manner. The whole chip is divided into six units and independent scan chains are constructed for each unit. Flip-flops (F/Fs) on the boundary of the unit are scanned so that the logic within the unit can be tested by its internal scan chains only.

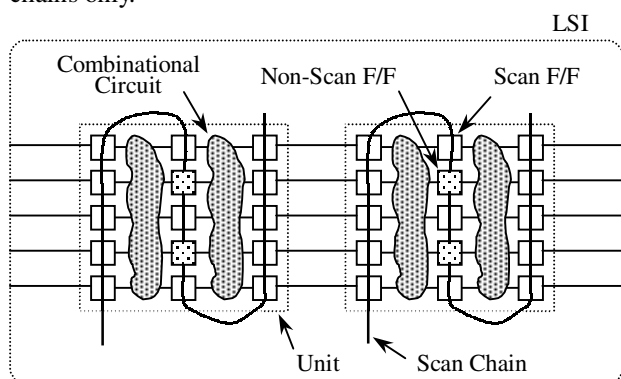


Figure 1. Scan structure

Two scan modes are provided for testing inside the units and for testing between them. Each unit is scanned separately in the former mode, while all the units are scanned at once in the latter.

This scan structure allows independent implementation of DFT and ATPG for each unit and thus shortens the test design TAT.

4. Scan Flip-Flop Selection

Scan F/Fs are determined manually by the designers to minimize the delay penalty in timing critical regions. However, the testability is automatically checked in a hierarchical way to find testability problems early in the design flow.

A static testability analysis tool is used to guide the scan F/F selection. The following three criteria are used in the testability analysis, which are experimentally known to be effective for test pattern reduction:

- The number of non-scan F/Fs between scan F/Fs
- The number of gates between scan F/Fs
- The number of scan F/Fs that fan-in to a scan F/F

The results of the scan F/F selection are as follows:

Scan F/Fs: 128k (53 % of all F/Fs)
Partial Scan Overhead: 1,670kTr. 7.5%
Full Scan Overhead: 3,170kTr. 14.3%(estimation)

5. Pattern Generation

Combinational ATPG is used in conjunction with sequential ATPG to minimize ATPG time and test patterns. A few manual patterns are added to test the timing critical circuits where no scan F/F is allowed.

Combinational ATPG is first applied treating all non-scan F/Fs as black boxes. Then, sequential ATPG is run targeting the remaining faults. This flow results in significant reductions both in the total number of generated patterns and in the total ATPG run time.

6. Conclusion

Several techniques for effectively applying partial scan DFT to a large high-speed system LSI have been shown. Advantages of the partial scan method are taken with these techniques while controlling its disadvantages, such as pattern length and ATPG time.