A practical logic BIST for ASIC designs

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1. Introduction

Increasing number of pins or gates in the latest LSI's requires a lot of testing resources. The conventional scan-based testing requires a costly tester (ATE) equipped with a lot of pin electronics. Since reducing the testing cost is a crucial issue in industry, we have introduced an approach using scan-based logic BIST to solve this problem. The logic BIST has applied to many ASIC design chips, which have up to several million gates.

2. Design Feature

The design feature of CMOS ASIC is as follows.

(1) Embedded gate array:

A chip has customized on-chip-RAMs, and the other area of the chip can be used for random logic. The capacity of a chip is 8 mega-gates when it is used for pure logic. This will enable the users to get a chip in a short production term.

(2) IO-interface:

More IO-pins can be available than which ATE has. Moreover, several kinds of IO-interface are usable. This will make it difficult to prepare functional test patterns through IO-pins.

(3) Clock design:

Gated-clock technique for a low-power design or multi-clock-domain is often used. Logic modification for DFT would be an elaborating work.

3. DFT (Design for Test) Method

We have applied a full-scan-based logic BIST for our ASIC testing. It has the characteristics as follows.

(1) Fault coverage:

Using a TPI technique and supplemental stored test [1] [2], most of the design chips attained high fault coverage of 99.5%.

(2) Logic design restrictions:

Using dedicated double clocks for testing, logic designs with few restrictions for testing were possible.

(3) DFT overhead:

A careful layout design of the DFT-circuits was done with the combination of DFT synthesis program and P&R program to reduce wiring overhead.

(4) Diagnosis:

A scan-based diagnosis program "KOGORO" was used [3].

4. Conclusion

Applying the DFT method shown above, the amount of test data was reduced to 10-100 times smaller than the conventional test (i.e. stored scan test). Thus, we could prevent an increase of additional investment cost for LSI testing.

The DFT overhead was also evaluated. The increase of the used gates was found to be less than 1% of the conventional scan-based logic.

Another advantage of logic BIST was an improvement of test quality. We evaluated it from various points of view [2]. To do this, a new delay-fault model, which considers delay values of defects and activated paths to detect them [4], was developed. From these evaluations, we could confirm the effectiveness of BIST for the various defects.

5. References

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