Panel I:
Mixed-Signal SoC Testing: Is Mixed-Signal Design-for-Test on Its Way?

Moderator & Organizer:

Chin-Long Wey
Michigan State University, USA

Panelists:

Adam Osseiran
Fluence (Europe), Switzerland

Jose Luis Huertas
IMSE, Spain

Abstract

The world market for electronic systems will reach $1 Trillion within a year and with further exponential growth over the next five years. The growth in areas such as telecommunications has increased the demand for creating single chip solutions to system. This has been achieved by integrating a number of complex sub-systems, including standard interface blocks (e.g., analog/digital converters), reused design cores (e.g., memory or microprocessors), embedded software, and new, innovative, custom designed "user blocks", into a single chip. Today, system-on-a-chip (SoC) has become a reality. However, the complexity of SoC makes it very difficult to achieve the desire test coverage without affecting the design schedule.

In the last decade, testing complex digital ICs has dramatically improved.

Fully automated test solutions are commercially available. DFT (design-for-test) and BIST (Built-in-self-test) methodologies have been well-developed and available for today's high-complexity and/or high performance designs. However, mixed-signal DFT is far behind. This is simply due to the lack of standard fault model for analog circuits, standard mixed-signal DFT methodology, and commercially available ATPG for mixed-signal circuits. A number of DFT and BIST design methods of analog modules, such as ADC, DAC, PLL, analog front end circuits, and etc., have been developed by university researchers. Due to high testing cost, many companies are still not willing to make efforts to perform testing on analog modules like embedded PLLs.

In order to improve SoC design productivity, efficient SoC test methods must be developed and commercially available. This panel will address the following interesting issues:

* Is toady's mixed-signal DFT methodology on its way to resolve the challenges of today's industrial market demanding?

* Is BIST the mixed-signal DFT solution?

* Is embedded test the mixed-signal test solution?

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