Challenges for the Academic Test Community

Melvin A. Breuer

University of Southern California
Los Angeles, CA- USA
mb@poisson.usc.edu

Abstract

These are exciting times for digital technology, as we see continual reductions in feature size and power supply voltage, and increases in chip size, density and speed. Unfortunately, test costs seem to demand an increasing fraction of the total production costs. Are we failing industry?

Over the last 20 years many active areas of research have emerged, such as ATPG, fault simulation, diagnosis, scan design, boundary scan, I_{DDQ} testing, delay and at-speed testing. In this talk I will focus on the academic contributions in some of these areas. I will address the question of whether researchers are targeting yesterdays problems, problems that industry will address in 1-2 years, or problems they will address in 5-10 years. Is most of our work incremental? Are we doing evolutionary or revolutionary research? As an example, we see a continual stream of papers on improving ATPG efficiency and test compaction? Are these the key problems in test pattern generation that need to be addressed? What about multiple clock domains, tri-state logic, bi-directional logic, dynamic logic, transistor primitives and latch-based designs?

At one end of the design spectrum designers have been using VERILOG and VHDL to describe their designs. Now signal processing engineers want to define their designs in C. How can we make these synthesized designs testable? Better yet, who is addressing the problem? At the other end of the spectrum, engineers are addressing low level issues such as noise (e.g. crosstalk), process variation and ground bounce. Is academia adequately looking at these problems?

Finally I will touch on the relationship between industry and academic research from the perspective of funding, sharing of data and distribution of software.

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Proceedings of the 9th Asian Test Symposium (ATS'00)
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