

Testing in the Fourth Dimension

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Abstract

Digital testing in the last three decades has taught us the value of design for testability (DFT). Disciplines such as scan and built-in self-test (BIST) have emerged as standard practices because they allow logic testing of arbitrarily large systems. This has been one of the greatest achievements in testing thus far. These past decades have also produced significant advances in semiconductor technology, which make extremely fine features and larger scales of integration possible. The beginning of the new millennium is an era of the system-on-a-chip (SOC). Today's specialized SOCs will soon become large-volume production chips and there will lie our testing challenge of the new millennium.

Those SOCs will contain mixed signal subsystems. Testing of analog parts has always required accurate generation and analysis of timing waveforms. Digital subsystems of the future SOCs can be characterized as ultra-high speed devices whose clock-rates will exceed any affordable automatic test equipment (ATE). Besides, the signal integrity of ATE to device under test interface will be a major source of yield loss. If we can learn from the experience of the past, DFT, though not necessarily the same DFT, should be the answer. I do not mean that a BIST-based speed test will have the ATE go away. I think the future design styles will explore new DFT methods for timing test that are similar to scan only in spirit. For example, high-speed clocks and other time-critical waveforms may be generated on chip by locally embedded circuitry (modified flip-flops, DSP, filters, etc.). So, the challenge for the future is to find a timing analog of "scan" that will allow both logic and timing tests of arbitrarily complex systems and also permit simple tests to ascertain the integrity of the DFT hardware.

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