

# **Built-In Self-Test for Analog and Mixed-Signal Designs**

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The trend of cramming more functionality onto a single chip poses alarming problems for testing and diagnosis. Complex chips such as those systems-on-silicon designs usually contain both digital and analog circuitry and include various cores from specialized design houses. Built-In Self-Test is an integrated test solution that could possibly hold down the soaring cost of external ATE machines for such complex chips. Even though in many large chips some form of BIST already exists, a complete, full-chip BIST methodology is still not available for mixed-signal designs. Mature BIST techniques for regular structures such as RAMs and ROMs are available and are being widely used. Techniques for random digital logic have been investigated for quite some time and vendors have begun to offer tools for implementing logic BIST structures and controllers automatically. Analog and analog/digital interface side has lagged behind and the design and test community has devoted more effort toward this direction over the past few years.

The potential of some BIST techniques for analog circuitry and converters in mixed-signal designs will be discussed. Some recently developed methods employ digital techniques and use the in-circuit digital logic to test the analog and interface circuitry. These methods embed an analog module under test between the chip's own D/A and A/D converters to form a digital-in digital-out module which can then be tested and analyzed by digital signals. By using proper test patterns and "signatures", the satisfaction/violation of the DUT against the specifications of the performance parameters can be determined cost-effectively. The speed of the D/A and A/D converters could be a limiting factor for testing high-frequency analog components under such methodologies. The challenges, opportunities, and possible variations of existing methods for high-frequency analog circuits will be addressed.