

## Challenges in Testing

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### Abstract

As technological advances in circuit design and manufacturing are made, testing procedures must accommodate diverse circuit description styles, large circuit sizes and new failure mechanisms. In this talk, we describe some of these challenges and how they are addressed in recent works in various areas of testing.

In recent years, the formulations of testing problems have changed from "given a problem, find a solution" to "given a problem and quality measures, find a high-quality solution". Quality guarantees provide ways to measure the distance between a given solution and an optimal solution. In addition they provide criteria for evaluating a new procedure that are more effective than for example comparison to previously proposed procedures. This is important when applying the procedures to very large circuits.

Recent works address testing issues at increasingly higher levels of the design cycle and offer an integrated treatment of design and test. High-level failure models are considered as well as solutions that are completely independent of a failure model. At the same time, failure mechanisms at the transistor level gain importance as design features are reduced. We describe some of these works and the advantages of the two directions.

Core or macro-based design consists of the incorporation of existing logic blocks (cores or macros) into a circuit. This design methodology reduces the time spent in designing the circuit. However, an embedded logic block may not be testable by a precomputed test set that ignores the environment where the block is embedded. Thus, macros-based design poses testing challenges that require existing testing methodologies to be reconsidered and new ones to be developed.

Recently, testing techniques have been extended to the more general problems of design verification and validation. The approaches to hardware design verification and validation can be classified as simulation-based or formal methods. Simulation-based approaches are incomplete and do not guarantee the correctness of a design. Formal methods are not easily scalable to large circuits.

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