New Research Problems in the Emerging Test Technology

Panel Discussion

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The panel will attempt to establish a list of relevant research problems in testing. To begin, each panelist will present two most important problems in testing. We will then invite comments from the audience. Initial thoughts of the panelists follow.

Bernard Courtois

Problem 1: *How high level design can cope up with realistic low level fault hypotheses?* The development of manufacturing possibilities leads to an ever increasing number of devices put on a circuit. To cope up with the complexity, the designer must work at higher and higher levels. But, faults actually occur at the layout (transistor) level. This leads to a large number of fault hypotheses. The main problem is that there remains a gap between the R&D steps in design and R&D steps in testing.

Problem 2: *How will microsystems be tested?* Twenty-five years ago the collective fabrication of devices on ICs made microelectronics a booming technology. Soon, the collective fabrication of microsystems will make microsystems a booming business. These microsystems will include mechanics, optics, chemical components, etc. They will possibly be 3-D packages and testing will be a challenge.

Fumiyasu Hirose

Problem 1: *Application of ATPG techniques to logic verification and synthesis.* Logic verification and synthesis have advanced through techniques like binary decision diagrams (BDD) and don't care (DC) sets, which are very efficient. However, because of memory explosion of BDDs, it is not necessarily robust against circuit size. On the other hand, since ATPG techniques are applicable to larger circuits, it should be very promising and efficient to employ them. The techniques include finding equivalent points between circuits under observability don't cares (ODC) and transforming circuits using redundancy addition and removal.

Problem 2: *Automatic system BIST generation from high level HDL.* Major macros, offered by the ASIC venders, considerably reduce logic design cost despite the explosion of transistor count on a chip. However, the cost of testing and test-design will become relatively larger. This problem should be solved by system BIST, and the implementation of BIST should be done from HDL and at a high level.

Sandip Kundu

The transistor count on a chip doubles every 18 months (Moore's law) and the performance also doubles every 18 months. Silicon Industries Association (SIA) has identified the microprocessor to be the technology trend setter for the next decade (as opposed to memory in the previous decade). So challenges in test are best understood in context of high performance microprocessor development: (a) chips will get bigger (20 million transistor on a chip by next year), (b) they will get faster (3ns or less), and (c) test technology may not keep pace with these trends.

Problem 1: Structural methods of testing (scan etc.) are increasingly becoming a problem because, (a) routing global wires add a lot of area overhead, (b) balancing a global wire for signal speed calls for solutions that are power hungry, and (c) greater than 50% of delay is contributed by interconnects. Forcing additional long interconnects (such as scan) increases the capacitance. On the other hand, the off chip interconnects on ceramic is getting

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relatively faster than the on chip interconnects through metal layers. To illustrate this point consider HP PA-RISC 8000 which has off chip single cycle cache. This technology trend will create an unprecedented opportunity for directly observing internal signals of a circuit. Thus, observation points for the internal structure of the circuit will not necessarily have to be outputs of latches. *Can we address test/DFT based on these observation points?*

Problem 2: Chips are getting bigger and balancing the clock tree (to adjust for skew at leaf nodes) takes a lot of power. At some future point people will look at locally balanced areas that talk to other areas of the chip asynchronously. Global scan is an unacceptable solution. *How do we do delay testing of asynchronous circuits?* By definition, asynchronous components are delay insensitive. How do we call a time out in asynchronous communication when there is no global reference point?

Chung Len Lee

Problem 1: *Testing and DFT for mixed analog-digital VLSI circuits.* Due to audio and video applications, more VLSI chips are fabricated in mixed mode. Previously, most efforts on testing and DFT were on digital circuits. Now there is an urgent need for testing techniques and design methodology for DFT for mixed signal VLSI circuits. Despite many difficulties, this area is rich in problems and offers numerous possibilities for innovation by test scientists and engineers.

Problem 2: *Testing and DFT for high density and high performance memory.* VLSI fabrication technology has advanced to a stage that memories of giga-bit density and nano-second access time can be fabricated. As testing on mega-size memories is already a very time-consuming and costly job, new testing techniques and DFT methodologies to efficiently and effectively test memories will definitely be welcome by the semiconductor houses.

Yinghua Min

Problem 1: *The gap between test technology and IC industry.* The development of test technology has been slow in the IC industry. The D-algorithm was published in 1967 when chips with thousands of transistors were produced. Now, microprocessors operating at 300 MHz with about 1 giga-transistors per chip have appeared, while CAD and CAT tools are adequate only for smaller chips with relatively lower speeds. Many challenges call for efforts on both basic research and technology application.

Problem 2: It is widely noticed that there are similarities between software design and IC logic design, and between software testing and IC testing. *We must explore such similarity and search for unified approaches.*

P. Pal Chaudhuri

Problem 1: *Coverage of structural faults with (weighted) behavioral test stimuli.* In addition to conventional approach of generating behavioral test stimuli, attempt can be made to include additional behavioral test stimuli based on specific structure that realizes the intended behavior. The sole objective of this approach would be to reduce overall test generation and test application time for a complex circuit.

Problem 2: *What can we learn from the human immune system to build next generation fault tolerant computers?* In response to external antigens, the immune system generates antibodies that aim to counter the antigens. A byte error on the datapath of a system can be viewed as antigens that can be countered with byte error correcting code circuit, selectively placed at the input and output of a functional block. Similar concepts can be developed for other types of errors. Contemporary ideas can be borrowed from the human immune system for cost effective design of fault tolerant computers.

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