

Synchronous Latency Insensitive Design

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Abstract

It has long been recognized that the on-going scaling leads to severe problems with wire delays, which eventually will become a showstopper for further scaling. Several methods to mitigate these problems have been suggested, maybe the most realistic one being the global asynchronous local synchronous (GALS) approach. In the same time we have learned how to manage system complexity through powerful methodologies, design flows and tools, based on the very successful paradigm of synchronous logic. The problem we face now is how to combine this successful paradigm with the need for mitigating wire delays. In this paper we will give a brief overview of on-chip interconnect properties and the wire delay crisis. We will shortly review various proposals to manage the wire delay problem. Finally we propose a new solution, Synchronous Latency Insensitive Design, which manages the wire delay problem without disturbing the synchronous paradigm. The new solution is a variation of the GALS approach, which accepts large variations in clock skew and data latency, is completely synchronous at RTL level, has a completely synchronous implementation and can be implemented with only standard digital library cells. The proposed approach can also be extended to multiple clock frequencies.