

High-Performance Front-End Signal Processors for Adaptive Sensor Arrays

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Abstract

Adaptive sensor arrays are being used for an increasing number of military and commercial systems including communications, radar, and sonar applications. The major goal of using adaptive techniques is to improve the system level performance by increasing signal-to-noise ratio, which is achieved by suppressing competing non-signal components such as interference, clutter, multi-path, circuit noise, and non-linearity. Increasingly complex algorithms are being adopted by these systems. The computational throughput requirement for some experimental systems can now exceed one trillion operations per second, with multi-quadrillion operations per second systems on the drawing board.

In order to meet the computational throughput requirements, highly specialized front-end signal processors have to be developed for these adaptive sensor array applications. Unfortunately, commercial off-the-shelf parallel DSP processors are usually suboptimal for such applications in terms of complexity, size, weight, power consumption, and cost. The adaptive sensor array signal processing algorithms tend to be continuous data flow type and not general decision based processing flow type. While commercial RISC and DSP processor architectures tend to be quite good at general purpose computing, significant die area and power consumption overheads are paid to handle general processing flow. Therefore, developing application specific architectures and processor technologies can significantly simplify the front-end processor and reduce size, weight, power, and cost.

In this talk, a number of application-specific front-end processor systems will be discussed including their processing algorithm, architecture, and processor implementation techniques. These front-end processors perform digital in-phase/quadrature frequency down-conversion, channel equalization, dynamic range enhancement, adaptive beamforming, space-time adaptive processing, interference nulling, and clutter suppression tasks. The computational throughput of these systems, which are being developed, range from hundreds of billions of operations per second to trillions of operations per second. The discussion will also include new system technology trends including direct RF sampling sensor systems, mixed signal front-end receiver/processor systems, and ultra-wideband frequency-channelized sensor systems.

Biography

Dr. William S. Song received his Ph. D., M.S., and B.S. degrees from Massachusetts Institute of Technology in 1989, 1984, and 1982 respectively. He has been working at MIT Lincoln Laboratory since 1990, and is currently a Senior Technical Staff Member in the Embedded Processor Systems Group in the Air Defense Technology Division.

During this time, Dr. Song has been working on high performance signal processor technologies for sensor array signal processing applications. He has developed numerous advanced signal processing algorithms and architectures as well as real-time embedded processor hardware implementations. Recently, he has been working on the scalable VLSI bit-level systolic array signal processor technology, developed for high computational throughput density applications with low power consumption requirements.

Dr. Song has been the technical director and project manager for a number of programs including the on-board signal processor for space based radar, high dynamic range digital receiver, digital beamformer processor, and miniaturized mixed-signal receiver/processor programs. His research areas also include wideband channelized signal processing, fault-tolerant computing, and high density mixed signal packaging.