

Computer Arithmetic – An Algorithm Engineer’s Perspective
(invited keynote)

David W. Matula
Professor of Computer Science and Engineering
Southern Methodist University
Dallas, USA
matula@enr.smu.edu

Abstract

The continuing evolution of hardware speed and expanding storage in cache and memory provides that the choice of fundamental arithmetic algorithms and numeric representations within the arithmetic logic unit must be continually addressed to obtain competitive arithmetic unit implementations. The ongoing expansion of the widely followed IEEE floating point standard particularly suggests numeric representation and algorithm choices to support a fused multiply-add, and possibly some quad precision capability, must be investigated. Algorithmic novelty is a priority both for competitive advantage and also to avoid being shut out by competitor’s intellectual property thrusts.

In this talk we identify some algorithmic goals for improving pipelined arithmetic unit performance including:

- reducing the dependent arithmetic operation penalty,
- reducing the rounding direction computation penalty,
- better integrating divide, square root, and reciprocal instructions into RISC design.

We describe promising research directions on algorithmic tools that can help attain these goals including:

- developing integrated arithmetic algorithms exploiting cost effective redundant representations within the arithmetic unit,
- utilizing concurrent table lookup concepts with supplemental small adders/multipliers to speed up iterative algorithms for divide, square root, and transcendentals.

The flexibilities available for algorithms in hardware provides a rich source for algorithm design of value both in theory and in practice.

David W. Matula received his Ph. D. from U.C. Berkeley in 1966 and has been a Professor of Computer Science and Engineering at SMU in Dallas since 1974. He has published over 100 refereed journal and proceedings papers and has 13 patents on arithmetic unit design and wireless network systems. He has been a consultant with Cyrix/National Semiconductor since Cyrix’s founding year, 1988, where he has contributed to the design of several generations of floating point units. He has had a paper at all 16 of the IEEE Arithmetic Symposia since their inception in 1969.