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Chip-level microarchitecture trends

..... One year ago, in introducing *IEEE Micro's* Hot Chips 14 special issue, I pointed out that features such as low power, reliability, security, and fault tolerance delivered to the customer at affordable cost might well serve as differentiating indices to the multidimensional entity called "system performance."

A year later, I cannot but overemphasize the emerging reality of that expectation. If anything, the focus on power dissipation as a primary design constraint has sharpened, with especially intense concerns about the static (leakage) component of power in future technologies. The basic uncertainty and variance of technology-related device and interconnect parameters (both across and within individually fabricated chips) that experts envisage are causing a major rethinking of the design stack (from high-level microarchitecture to physical design and layout). In addition, there are major implications in terms of design tool support for future, technology-aware microprocessor development.

This year, the Hot Chips 15 special issue is guest edited by Michael Flynn and Pradeep Dubey. Their guest editors' introduction covers the articles selected for publication in *IEEE Micro*. One of the trends in high-performance microprocessor chips is the increased level of on-chip integration that the technology has made available. IBM's Power4 had previously started the trend of multicore designs with a dual-core chip multiprocessor offering.

This issue of *IEEE Micro* includes an article on the follow-on chip called Power5, still a dual-core solution, but with each core supporting two independent program threads for a total of four concurrently executing threads per chip. Recent announcements by other vendors depict a similar trend, with an increasing emphasis on enhancing chip-level throughput through multiple cores and threads. In these future designs, each core or thread may not necessarily aim at delivering the highest frequency or performance that is achievable for the given technology.

The power "wall" is definitely a factor that could accelerate this trend, since single-core frequencies might not scale up to meet prior trends. On the other hand, the chip-level power and area budgets (especially pertaining to leakage) place a natural limit on the number of cores for a given level of core complexity. This leads to some interesting power-performance tradeoffs that would balance single-thread performance against targets for chip-level throughput, working within a given power and cost budget. Yield and reliability aspects of the design equation (in an era of technological uncertainties) make the future space of design choices even more interesting!

Of course, in some markets, single-thread performance might remain the primary driver of chip-level microarchitecture design. Here, to meet performance targets at affordable cost, cooling and pack-

aging technologies must improve sufficiently to meet the challenge.

I hope you enjoy reading the leading-edge articles in this special issue. They capture some of the latest advances, trends, and challenges in microprocessor design.

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