



MICRO'S TOP PICKS FROM MICROARCHITECTURE CONFERENCES

Charles Moore
The University of Texas
at Austin

Kevin W. Rudd
Intel

Ruby B. Lee
Princeton University

Pradip Bose
IBM T.J. Watson Research

..... *IEEE Micro* focuses on contemporary design issues facing chip and hardware system designers. We publish in-depth descriptions of new or soon-to-be-announced designs from the industry to highlight both the design and the design issues addressed. As a result, *IEEE Micro* is a very important source of information on a wide range of processor techniques used in the industry today.

As many readers are certainly aware, there are several important computer architecture conferences each year where researchers from academia and industry present papers that describe emerging issues and propose new ideas for addressing them. We thought that it might be interesting to identify representative "Top Picks" from these conferences over the past year, based on their industry relevance and interest to the largest possible segment of *IEEE Micro's* readership. This would give more visibility to these ideas, facilitate potential industry adoption, and provide wider recognition to the authors.

We invited the selected papers' authors to submit essentially the same paper on the same ideas, allowing updates on only minor new work done since the conference publication, along with rewriting and editing to tailor it to *IEEE Micro* audiences. Because of the abundance of excellent submissions and shortage of space, we invited some as short articles,

where the authors had to significantly condense their original work.

As you might expect, it is difficult, even risky, for us to try to identify which papers represent the "top" ones and which might have the biggest impact on future industrial designs. Essentially, every submission we received represented excellent ideas, since each submission had already been selected and carefully peer-reviewed for a highly selective architecture conference. Each submission also represented an immense amount of thought and effort by an author or team of authors.

Although quantitative approaches have been advocated and widely used in research as a means for identifying promising ideas, there is still an art to computer architecture that you simply cannot quantify. In recognition of this fact, we allowed our review process to include some amount of qualitative assessment. As a result, these selections reflect our impressions of the work, and are only a very small set of representative "top" ideas. There were many excellent submissions that we did not have the space to include. In addition, we only considered work that that authors had described in a submitted abstract in response to our call for submissions, so it is also highly likely that there are some great ideas out there that this issue does not cover at all.

Review process

The call invited submissions on work published at any IEEE or ACM architecture conference between October 2002 and December 2003. It required the submissions to be abstracts, a few pages in length, describing the technical contributions along with statements about the work's potential industry relevance and why *IEEE Micro* readers would be interested.

In response, we received 72 submissions from papers originally published in the following conferences:

- International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-X 2002),
- Annual International Symposium on Microarchitecture (MICRO-35, 2002),
- Annual International Symposium on Computer Architecture (ISCA 2003),
- International Symposium on High-Performance Computer Architecture (HPCA 2003),
- International Conference on Parallel Architectures and Compilation Techniques (PACT 2003),
- International Conference on Computer Design (ICCD 2003), and
- Annual International Symposium on Microarchitecture (MICRO-36, 2003).

A subset of the editorial board read and reviewed all submitted abstracts. Those that received high marks on the numerical assessment or at least one "top 10" vote went out to an extended review team that included other editorial board members and other experts in the field. These additional reviews were used to select the "Top Picks" published in this issue. Throughout the process, conflict-of-interest situations, including authors from the same institution, were handled according to IEEE conference review rules, where the other review committee members who did not have a conflict of interest made decisions about an affected paper. Also, the editor in chief and associate editor in chief stipulated a ruling in which papers coauthored by either of them would not be eligible for consideration in this special issue.

The Top Picks

With much difficulty, we selected 15 papers that cover a wide range of topics. Some were invited as regular length articles, others as short articles. They all contain interesting and promising ideas.

We hope that they inspire you to read the original work, contact the authors, and perhaps even spark some connections with design issues that you are working on.

Here, we give a loosely categorized breakdown of Micro's Top Picks.

Building on conventional microarchitectures

- "Checkpoint Processing and Recovery: An Efficient, Scalable Alternative to Reorder Buffers"
- "Runahead Execution: An Effective Alternative to Large Instruction Windows"

Unconventional architectures

- "The Jrpm System for Dynamically Parallelizing Sequential Java Programs"
- "Scalable Vector Processors for Embedded Systems"
- "Exploiting ILP, TLP, and DLP with the Polymorphous TRIPS Architecture"

Power- and temperature-aware design

- "Temperature-Aware Computer Systems: Opportunities and Challenges"
- "Dynamic Frequency and Voltage Scaling for a Multiple-Clock-Domain Architecture"

Reliability

- "Measuring Architecture Vulnerability Factors"
- "Transient-Fault Recovery for Chip Multiprocessors"

Performance analysis

- "Discovering and Exploiting Program Phases"
- "Addressing Workload Variability in Architectural Simulations"

Cache, memory, and multiprocessor optimizations

- "Nonuniform Cache Architectures for Wire-Delay Dominated On-Chip Caches"
- "Token Coherence: A New Framework

- for Shared-Memory Multiprocessors”
- “Transactional Execution: Towards Reliable High-Performance Multithreading”
- “Speculative Synchronization: Programmability and Performance for Parallel Codes”

We hope that you enjoy this special issue of *IEEE Micro*. It turned out to be one of the most challenging issues to pull together. This is our first attempt at an issue selecting Top Picks from architectural conferences; we will hone the process for next year, and welcome any constructive suggestions or comments you might have.

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Charles Moore is a senior research fellow at The University of Texas at Austin. His previous experience includes 18 years at IBM, where he was a Distinguished Engineer, a member of IBM's Academy of Technology, and a Master Inventor. He was the chief engineer for the Power4 chip, and the PowerPC 601 microprocessor. His current research interests include virtualization in system architecture, polymorphic computer architectures, and design verification. Moore has a BSEE from Rensselaer Polytechnic Institute and an MSEE from The University of Texas at Austin. He has 18 patents in various aspects of microprocessor and bus design. He is a senior member of the IEEE and a member of the ACM.

Kevin W. Rudd is a senior computer architect, Enterprise Processors Division, Intel Corp. He is responsible for investigating directions for future Itanium microarchitectures and providing Itanium processor architectural support to project teams and other internal and external users. His research interests include instruction-level parallel processors, especially efficient, high-performance architectures; application of software-engineering techniques to improve hardware design; programming languages and systems; and the hardware-software interactions and tradeoffs of various compiler techniques. Rudd has a BS,

MS, and PhD in electrical engineering from Stanford University. He is a member of the IEEE, the IEEE Computer Society, and the ACM.

Ruby B. Lee is the Forrest G. Hamrick Professor in Engineering and a professor of electrical engineering, with an affiliated appointment in computer science, at Princeton University. She is also the director of the Princeton Architecture Lab for Multimedia and Security, where her current research is in architecture for more pervasive cyber security, including designing security into processors and core software. Previously, she was the chief architect at Hewlett-Packard, leading interdisciplinary projects in processor architecture, multimedia architecture and security architecture, including the definition and evolution of the PA-RISC architecture and MAX (the initial general-purpose multimedia instructions for microprocessors). Lee has an AB with distinction from Cornell University, an MS in computer science and computer engineering, and a PhD in electrical engineering, both from Stanford University. She is a fellow of the IEEE, a fellow of ACM, and a member of SPIE, Phi Beta Kappa, and Alpha Lambda Delta. She holds 115 US and international patents.

Pradip Bose is a research staff member and manager at the IBM T.J. Watson Research Center; he is also editor in chief of *IEEE Micro*. His earliest work at IBM was on the Cheetah/America RISC superscalar processor, a project mentored by industry pioneer John Cocke. His current research interests include high-performance computer architectures, power- and complexity-aware design, and computer-aided design. Bose has a PhD in electrical and computer engineering from the University of Illinois, Urbana-Champaign. He is a senior member of the IEEE and the IEEE Computer Society, and a member of the ACM.

Direct questions and comments about this special issue to Pradip Bose, IBM T.J. Watson Research Center, PO Box 218, Yorktown Heights, NY 10598; pbose@us.ibm.com.