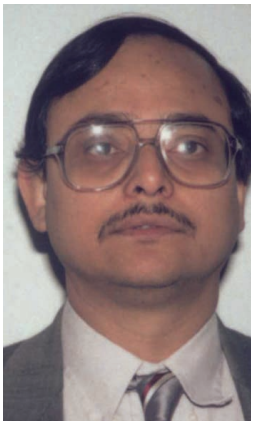

Design and integration: Chip- and system-level challenges

Pradip Bose
pbose@us.ibm.com

In this special issue, guest edited by Alberto Sangiovanni-Vincentelli and Luciano Lavagno, the readers get an excellent view of the issues, challenges, and trends in on-chip integration within the emerging field of complex system-on-a-chip (SOC) design.

These articles come from presentations at a Project Madess workshop in Rome. Madess stands for Materiali e Dispositivi per l'Elettronica dello Stato Solido (materials and devices for solid-state electronics); it is a special initiative managed by Italy's Council of National Research (CNR). An ambitious multiyear project, Madess has sought to promote the cooperation of industry and academia in microelectronics development (http://www.madess.cnr.it/summary.htm). These articles cover challenges presented by

- using SOCs in automotive applications,
- integrating the wide variety of functionality in future SOCs for consumer electronics,
- manufacturing gigascale SOCs, and
- integrating SOCs with microelectromechanical systems (better known by their acronym, MEMS).

Of all of these, the most pervasive yet transparent use of SOCs occurs in automobiles. A typical, state-of-the-art automobile in 2003 is already equipped with dozens of embedded processors or controllers to control navigation, comfort, safety, and entertainment. What additional features are in the offing? And what new developments, trends, and uncertainties in system design can either hasten or deter these future automotive trends? What, indeed might future automobiles look like, in view of the anticipated challenges and capabilities of the embedded electronics? This article certainly opens our minds to new challenges and opportunities in the always-exciting world of automobile design.

Other articles outside the guest-edited issue also address SOC design. Richardson et al. describe the implementation of a high-speed (520 MHz) synthesized CPU core. Such cores, of course, are typical computing elements within a larger SOC. The article by Amaury Nève, Denis Flandre, and Jean-Jacques Quisquater shows a promising application of SOI (silicon-on-insulator) technology in the domain of future smart cards.

I hope you enjoy reading the articles in this exciting new issue of *Micro*. Please e-mail the editorial board and me with your comments and suggestions. Even if you cannot contribute articles, please do let us know what future topics you would like *Micro* to address.

Best Student Paper Award at ISCA

The International Symposium on Computer Architecture met in June this year, as part of the larger 2003 Federated Computing Research Conference, FCRC (http://www.acm.org/fcrc/). *IEEE Micro* and ACM SIGARCH are proud to have cosponsored a best student paper award at ISCA, dedicating this award to the memory of Bob Rau, pioneer VLIW microarchitect (Micro News, Jan.-Feb. 2003). The winning paper (as selected by the ISCA program committee) is "Temperature-Aware Microarchitecture" by Kevin Skadron, Mircea R. Stan, Wei Huang, Sivakumar Velusam, Karthik Sankaranarayanan, and David Tarjan.

Micro congratulates all the coauthors—students and professors—of this excellent paper, which deals with devising microarchitectural techniques for mitigating the problem of temperature hot spots. Resulting from increasing levels of power density within specific units in a microprocessor, hot spots are an increasing problem, so this paper covers a timely topic.

Micro will attempt to include a summary of the key technical highlights (talks and panels) presented at ISCA in its July-August issue. It also plans to track the key highlights of other relevant conferences held this year, in particular Hot Chips, Microprocessor Forum, the International Symposium on Low-Power Electronics and Design (ISPLED), and, of course, the International Symposium on Microarchitecture (MICRO-36). As previously announced, *Micro* will attempt to bring you revised and adapted versions of the best work published in the leading architecture conferences in its year-end special issue.

0272-1732/03/$17.00 © 2003 IEEE Published by the IEEE computer Society