

Manufacturing test woes



■ **WITH THE MANUFACTURING CAPACITY** of thousands of wafers per week, and thousands of dies per wafer, today's silicon comes out of fab really fast—and furious—sporting device I/Os in the gigabit-per-second range. But it is increasingly going into high-volume and low-cost consumer electronic parts, exhausting the available time and money to test these parts. Little wonder that the 2003 *International Technology Roadmap for Semiconductors (ITRS)* lists the high-speed interface to ATE as the number one test challenge.

To be sure, high-speed differential links have been with the industry in communications ICs for a long time, even as communication links move to 10-Gbps speeds in the short haul (backplanes) and 40 Gbps in the long-haul links. What has changed, however, is the recent proliferation of high-speed serial protocols into diverse (and mainstream) processors, ASICs, and SoCs. It is not uncommon to see ASICs with serial interfaces operating at over 3 Gbps, rapidly approaching over 10 Gbps. These ASICs are driven by serial communications and backplane standards such as PCI Express, RapidIO, and HyperTransport—all of these advancing to over 5 Gbps. Suddenly, a part designed for low-cost manufacturing requires manufacturing test solutions that are still dominated by expensive and time-consuming test equipment designed for at-speed functional testing, diagnosis, and debugging. The situation becomes worse: Many of these devices sport multiple high-speed serial interfaces, requiring multiport ATE solutions. But the same economics requires the manufacturer to minimize manufacturing yield losses from test equipment shortcomings and test inaccuracies.

For an industry accustomed to planned equipment upgrades, these changes produce many red brick walls, that is, problems with no known solutions. One of these nasty problems is jitter measurement and analysis in ATE. Jitter measurements must account for and dis-

criminate between deterministic and random jitter. A 10-Gbps digital signal has substantial spectral components at the second and third harmonics. Thus, jitter measurements at very wide bandwidths are necessary. For these measurements, jitter accumulation time is typically too high (at tens of seconds), requiring intelligent clock recovery and handling to make it usable for manufacturing test. To be effective in combating yield loss, the test equipment must accommodate the use of forwarded clock and self-timed data streams that might have drift well in excess of bit duration. Although the concept of multiple bit length channels comes naturally to communication system designers, it is a difficult one for test equipment manufacturers accustomed to synchronous bit spitting in the consumer CMOS markets. Testing for jitter tolerance requires ATE solutions that can inject jitter into the data stream. Although diagnostic test solutions fill the gap in the short term, in the longer term, designers must engage DFT features or extend them to include performance-oriented parametric coverage, such as jitter measurement, to help manufacturing test. Naturally, as test complexity increases, some of the test infrastructure will land inside the chip as part of enhanced DFT. This is a topic that *Design & Test* considered in a special issue on Infrastructure IP (May-June 2002). Later, in the September-October 2003 issue, *D&T* covered at-speed test and binning, looking at how to distinguish between delay problems from manufacturing variations versus those from random effects. Guest editors André Ivanov, Fabrizio Lombardi, and Cecilia Metra expertly put together the current issue, which takes an in-depth look at the testing issues in the multiGbps regime with articles on test interfaces, and jitter models and measurements.

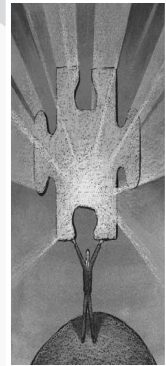
Recently, the editorial board and I concluded our daylong meeting with a focus on possible themes for the coming year. I am pleased to report that a very

active editorial board generated more than a dozen concrete proposals on exciting themes ranging from 3D integration, design for manufacturability, and nanoscale technologies, to configurable computing, chip multi-processors, and networks on chip. We continue to look for new ideas and suggestions on technical topics that interest our readers. Please do drop us a suggestion or comments if you would like to see any specific topic covered in *D&T*. Once again, I sign off with the hope that you enjoy this issue!



Rajesh Gupta
 Editor in Chief
IEEE Design & Test of Computers

**Help shape
 the IEEE
 Computer
 Society of
 tomorrow.**



Vote for 2005 IEEE

Computer Society officers.

Polls open 13 August – 4 October

www.computer.org/election/



Correction

In the May-June 2004 issue—in the article “Reconfigurable Architecture for Autonomous Self-Repair” by Subhasish Mitra, Wei-Je Huang, Nirmal R. Saxena, Shu-Yi Yu, and Edward J. McCluskey—an incorrect image appeared in Figure 2, p. 229. The correct version is reprinted here. *IEEE Design & Test* regrets this error.

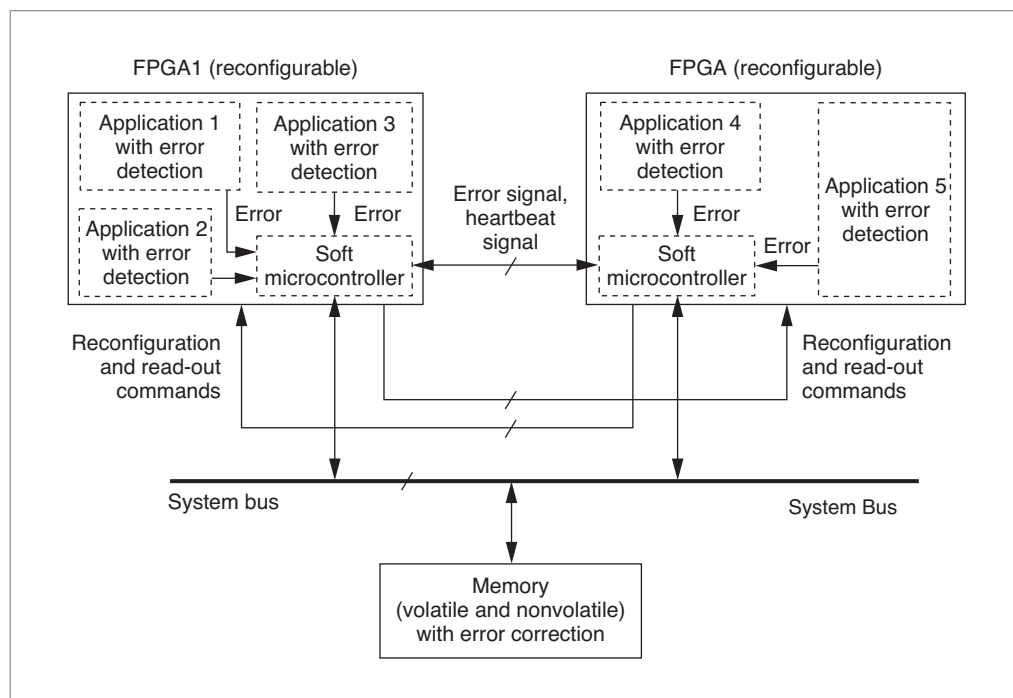


Figure 2. Dual-FPGA architecture.