

From the EIC

The next EDA challenge: Design for manufacturability



■ **OVER THE PAST DECADE**, innovations in IC design methods have managed to successfully separate semiconductor manufacturing from the overall IC design process—so much so that these innovations made possible a whole industry of fabless design houses and its foundries. It seems now that many of the past challenges are coming home to roost and slowing down the adoption of new process nodes, reminding us all that IC design is primarily a manufacturing miracle—one where product engineering and manufacturing issues rule the roost.

However, in at least one significant way, the IC design process has qualitatively changed from vertically integrated design houses: electronic design automation (EDA) and its industry are now a significant part of the creative equation to successfully design and manufacture IC parts. The key to successfully navigating these process technology challenges is a complete overhaul of the design flow. Such an overhaul must include reliability and manufacturing concerns as an integral part of the design agenda, and incorporate the support of tools, throughout the design process. In his keynote address at DAC last year, Alberto Sangiovanni-Vincentelli identified design for manufacturing (DFM) as one of today's key EDA technology drivers. Although nanometer process technology issues dominate the DFM agenda as new challenges arise for evolving process nodes, the diversity of demands placed on process technology poses another challenge. That's because the diversity of new industry segments in embedded systems, sensors, flat-panel display controllers, CMOS image sensors, microelectromechanical systems (MEMS), and radio frequency identification (RFID) parts do not necessarily push the technology node in lithography dimensions alone, but instead place diverse demands on (commoditized) processes.

There is an increasing awareness that each phase of the modern system-on-chip realization flow—from design to manufacture, test, assembly and packaging—impacts manufacturing yield and field reliability. To optimize yield and reach acceptable SoC reliability levels, the semicon-

ductor industry is beginning to employ solutions implemented at the design phase and used at different phases of the design flow. Our guest editors, Dimitris Gizopoulos and Yervant Zorian, have carefully put together this special issue of *Design & Test* to present different types of DFM techniques and their importance to yield optimization and field reliability. The articles in this theme examine areas such as design-manufacturing interface, impact on synthesis for manufacturability, DFM in embedded memory, logic, defect tolerance, and using reconfigurable circuits for autonomous self-repair. Our nontheme articles address advances in delay fault testing for nanometer multigigahertz designs.

This issue is also special in that it highlights *D&T's* relationship with the Design Automation Conference (DAC). Over the years, DAC has become the premier host for presentations on advances in EDA and its impact on IC design. This issue presents a preview of DAC items that our readers will find of interest. In the July-August issue, we will publish highlights of the DAC program and its buzz, including our popular *D&T* roundtable discussions.

With this issue, I am pleased to announce the addition of Seth Copen Goldstein and Sandeep Shukla to our editorial board. Seth will be area editor for nanotechnology architectures and design technology; and Sandeep will be area editor for system specification and modeling. I am also pleased to welcome Hidetoshi Onodera to our *D&T* Alliance Program as Asia liaison, a role he takes over from Kenji Yoshida. Our sincere thanks go to Kenji for his years of service on the DTAP program. With these exciting additions to the editorial board, we continue to strive to bring the most interesting technical developments to our readers. I hope you enjoy the issue.

A handwritten signature in cursive script that reads "Rajesh Gupta".

Rajesh Gupta
Editor in Chief, *IEEE Design & Test of Computers*