

Past successes, future challenges



■ **THIS ISSUE** marks the completion of 20 years for *IEEE Design & Test!* These 20 years have been filled with excitement for the semiconductor industry. The technologies covered in *D&T*—whether VLSI design or manufacturing test—have routinely plowed through challenges in semiconductor processing, devices, and circuits and systems design. This remarkable growth has outpaced even the most optimistic projections on technological capabilities—as documented in painstaking details in the *International Technology Roadmap for Semiconductors (ITRS)*. *D&T* has been proud to be at the forefront of this technological evolution, examining in necessary technical depth the most relevant and pressing issues in microelectronic IC and systems engineering.

As the editorial board and I look back and think forward, we find a future just as promising, yet holding many challenges where past lessons might or might not apply. Once again, North America seems to be losing its manufacturing base to large-scale, patient, and low-labor-cost investments made overseas. The situation is not unlike that of the early 1980s when, after six years of consistent decline, the US semiconductor industry had lost its leadership to Japan by 1985. At a time in which the future looked bleak, the Semiconductor Industry Association, with the help of a supportive Reagan administration, built the SEMATECH consortium that became the driver for several innovations in the precompetitive space of equipment manufacturing for semiconductor companies. Without doubt, the US investment of roughly \$800 million contributed to the technological advances and expansion of the US semiconductor industry, which now represents about 6% of the manufacturing gross domestic product (GDP). Semiconductors is the largest value-added industry in manufacturing, larger than the iron and steel, and motor vehicles industries combined. More importantly, the semiconductor industry has been a major patron of high-technology talent and a generator of high-wage jobs.

The US semiconductor industry now faces a different time and a different challenge—but once again, its fate remains tied to the actions of US industry leaders and policymakers. Even as semiconductor manufacturing moves overseas—this time a movement that the US industry, rather than foreign competitors, is driving—the proliferation of silicon chips into new application domains continues to grow unabated. However, the new semiconductor industry, with its unique set of technology challenges, is radically different from the high-volume silicon manufacturers of the past. The new semiconductor is often application-specific and relies heavily on software and reuse of diverse intellectual property to achieve its system-level goals. From the few high-volume parts of the past, the industry is rapidly disaggregating into many specialized application areas. The Fabless Semiconductor Association lists at least 72 application markets that rely on high-value IC designs, and more than 75% of these markets have a total market size of less than \$1 billion. In an era of sophisticated commodity manufacturing, a semiconductor company's access to its own manufacturing facilities is no longer a competitive advantage. Indeed, the challenge has now shifted to architectures and designs, as the ability of companies to manufacture complex chips exceeds their ability to correctly design these parts within rapidly shrinking time windows.

Once an afterthought, design verification now dominates the time and investment in high-value semiconductor parts. This issue focuses on the interplay of functional verification and manufacturing test. The efficient generation of a good test vector set is important to both. Guest editors Magdy Abadir and Li-C. Wang have carefully put together a special issue with articles that examine advances in automatic test vector generation, practical advances in formal verification, and their use in microprocessor designs. This is the first of two issues on design verification scheduled for this year. Later in the

year, *D&T* will focus on the synergies between different verification techniques—from simulation to various types of formal verification—and their overall fit within the design flow.

We celebrate our 20 years with a perspective article on the history of *D&T* by its founding editor in chief, Roy Russo. In the coming issues, we will feature articles from our past EICs, in chronological order, reflecting on the pressing issues of the times and their implications on the future.

I am also pleased to announce several editorial board appointments: Michael Nicolaidis of iRoC Technologies joins us as area editor for Defect and Fault Tolerance; Bruce Kim of Arizona State University joins us as area editor for Microelectronic IC Packaging; André Ivanov of the University of British Columbia joins us as area editor for Infrastructure IP; and Sani Nassif of IBM joins us as area editor for Deep-Submicron IC Design and Analysis. After serving as area editor for Defect and Fault Tolerance, Dimitris Gizopoulos will now focus his energies on building a department on Design for Manufacturing, Yield, and Yield Analysis.

I also thank Peter Ashenden for his excellent contributions to the Standards department, which will now be edited by Victor Berman, an EDA industry veteran of more

than 20 years. I thank Paolo Prinetto and Ahmed Jerraya for their service to the editorial board. Paolo will now be editing the TTTC Newsletter, and Ahmed joins the *D&T* Alliance Program as liaison for the DATE community. Finally, we are honored to have Tom Williams of Synopsys join the advisory board in setting long-term editorial policies for *D&T*.

The *D&T* editorial board and department editors are among the leading experts in their domain and industry, and are dedicating themselves to continuously supply valuable technical content to you, the magazine's readers. Working with them is an honor and a pleasure for me, exceeded only by your participation and interest as a reader and evaluator of the content we put together for every issue. We look forward to your feedback and suggestions as we continue to tune *D&T* to meet your needs for important technical information.



Rajesh Gupta
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Correction

In the January-February 2004 issue—in the article “Seamless Test of Digital Components in Mixed-Signal Paths” by Sule Ozev, Ismet Bayraktaroglu, and Alex Orailoglu—an error occurred in Table 3, p. 52, where several mathematical symbols appeared incorrectly. The correct version is reprinted here. *IEEE Design & Test* regrets this error.

Table 3. Tests at the module boundaries for selected parameters, where f , f_1 , and f_2 represent input signal frequencies; p and b are parameters describing the behavior; A_{in} , A_{in1} , and A_{in2} are amplitudes of the corresponding signal tones, and A_{max} is the maximum allowable input amplitude.

Parameter	Ideal test inputs
P_{1dB}	$f \in pb$ $A_{in} = P_{1dB(min)}$ One-tone signal
IIP_3	$f_1, f_2 \in pb$ $A_{max} - 20 \text{ dB} \leq A_{in1}, A_{in2} \leq A_{max} - 6 \text{ dB}$ Two-tone signal
f_c	$f_1 \in pb, f_2 = f_{c(min)}, f_3 = f_{c(max)}$ $A_{max} - 25 \text{ dB} \leq A_{in1}, A_{in2}, A_{in3} \leq A_{max} - 10 \text{ dB}$ Three-tone signal
DNL	$f_1, f_2 \in pb$ $A_{in1}, A_{in2} = A_{max} - 6 \text{ dB}$ Two-tone signal