From the EIC

Predictability in design and manufacturing

PREDICTABILITY in function and performance is important to semiconductor IC design. It is fundamental for continued integration of system parts onto the chip and crucial to decisions concerning substantial investments in chip design projects. So far, determinism and static analysis of the circuit blocks have guaranteed predictability. Indeed, from the early days of Spice, advances in IC design and integration have been fueled by the designers' ability to correctly simulate and predict circuit behavior. The designers have even accounted for the process variations in a deterministic way, that is, through simulation across process corners.

The new process nodes in the sub-100-nanometer domain, however, present a challenging design and test environment. A combination of variations in device parameters and coupling effects in the interconnect produces device behavior with significant variability in timing, drive, leakage, and so forth. Statistical variation and analyses are increasingly a part, not only of manufacturing, but also of the design process. Physical-level design is at the forefront of dealing with such design for manufacturability issues. Recent efforts in physical design tasks aim to incorporate the growing device and process variations. These include cell/module selection, cell placement, sizing, and routing. However, beyond these individual tasks, the overall process used for physical design also directly affects the quality and manufacturability of the IC chip.

This issue of *IEEE Design & Test* features a special section on advances in RTL to GDSII, diligently put together by our guest editors, Dwight Hill and Andrew Kahng. The focus in this section is on the integration of tools and tool flows (in other words, handling of data across tools); and on timing closure in the design process. The title itself, RTL to GDSII—From Foilware to Standard Practice, justifiably implies a sense of direction and the importance of design flow. However, it is not just the RTL that goes into the physical-design process. It also involves all the libraries, models, and physical constraints before a design converges to its final implementation. The two articles in this section, "An Integrated Environment for Technology Closure of Deep-Submicron IC Designs," by L. Trevillyan et al., and "Crosstalk-Aware Placement," by J. Lou and W. Chen, deal with these problems.

In addition, this issue features two articles addressing the speedup of manufacturing test. In an article on methods for setting up test equipment, Lin et al. describe efficient wafer probing to speed up the testing process. Complementing this, an article by S. Ozev et al. illustrates a method for reducing DFT overhead when handling mixed-signal circuits. In another nontheme article, N. Sirisantana and K. Roy describe techniques to minimize power consumption through the accurate selection of threshold voltage, channel length, and oxide thickness.

In this first issue of our 21st year of operation, I am proud to outline an exciting set of special issues planned for the year. These include topics ranging from functional verification, design for yield, and high-speed testing, to multimedia in embedded systems. As always, your suggestions on topics of interest are very welcome.

With this issue, I would also like to welcome Anna Kim, our new editorial assistant, to the *Design & Test* staff. Anna comes to D&T with substantial experience in handling technical articles and their presentation for a wider audience. Welcome, Anna!

Rajesh Gupta

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