Guest Editors' Introduction: Speed Test and Speed Binning for Complex ICs

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SPEED IS CRUCIAL for today's semiconductor products and can be a differentiator among suppliers vying for the same market. Of course, the first step is to design the product with the performance requirements in mind. But the second step is equally important: testing and characterizing the device to guarantee that it fully meets customer performance expectations. Conducting this testing thoroughly for complex devices fabricated in deep-submicron (DSM) designs—now in the neighborhood of 130-nm technologies and below—is becoming increasingly more difficult. But it's not just microprocessor manufacturers that are using at-speed tests these days. Increasingly, more manufacturers of all types of ICs are aggressively moving to add at-speed tests to their portfolio.

This special issue focuses on the important problem of speed test and speed binning of digital ICs. Topics in this issue span the entire design and fabrication process of an IC, from initial design through production test and characterization.

First, Intel's Kee Sup Kim, Subhasish Mitra, and Paul G. Ryan provide a comprehensive survey of delay testing techniques for high-performance designs. They begin by presenting manufacturing data to illustrate the necessity of delay testing. In particular, they show that 500 parts per million would not be achievable without delay testing. They then discuss how to differentiate between delay problems due to manufacturing variations and those from random defects. Any strategy for speed binning must consider random defects. Moreover, a structural test strategy, even running at a lower speed, can still play an important role in screening random delay defects. Finally, they discuss two important issues in structural testing: avoiding the adverse impact of a time-borrowing design style on signal propagation, and delivering test patterns with compression for test memory reduction. For speed binning of high-performance parts, high-quality transition fault testing is necessary, and structural delay testing requires a careful design of clock schemes to avoid potential yield loss.

Next, Xijiang Lin et al. from Mentor Graphics discuss improved features in an ATPG tool for structural delay testing. They begin by discussing how to use on-chip phase-locked loop (PLL) clock generator circuitry to create at-speed scan patterns. They provide a detailed example to illustrate how to model a PLL in the ATPG tool, and how to devise the clock scheme in at-speed scan testing. They then propose an approach that combines stuck-at and transition fault tests to improve test quality and reduce tester memory requirements. The goal is to achieve a desirable stuck-at coverage level with reasonably high transition fault coverage. The second half of the article presents a case study of a large industrial design. The authors classify transition fault coverage within each clock domain and between clock domains, and they discuss combining stuck-at and transition fault tests. They conclude that using an on-chip clock generator for at-speed structural test is cost-effective.

In the third article, LogicVision's Stephen Pateras describes BIST implementation techniques to achieve structural at-speed testing, and he addresses important timing setup issues from a logic BIST perspective. These issues can occur at the interfaces between a logic BIST controller and scan chains, or between flip-flops in different clock domains. There are also timing issues in distributing the scan-enable signal, handling multicycle paths, and dealing with different frequency domains. Pateras proposes logic-BIST-based techniques to address each timing issue. He concludes that logic BIST is a field-proven approach for at-speed structural test applications.

Next, Al Crouch of Inovys Corp. addresses the prag-

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matic application of structured delay tests. This article's scope stretches all the way from early design (how to set up the environment for static timing analysis) to post-silicon (how to debug design timing by using various structured delay tests). Crouch addresses the question of when to use transition versus path delay tests, and he illustrates a practical procedure for ranking paths and selecting those for which either type of test generation is appropriate. Coverage, particularly path coverage, is another important question that he addresses in the context of a proposed overall test generation flow that relies on handshaking between various design tools. This flow emphasizes intelligent path selection and test generation that occur in parallel. Crouch addresses layout aspects and their effect on path length and criticality. He provides examples of debugging situations, and he summarizes the proposed system's effect on ramping a new design.

In the fifth article, Bruce Cory, Rohit Kapur, and Bill Underwood represent a joint experimental work between nVidia and Synopsys. In today's industrial practice, it is important to ask whether it's possible to remove functional test's dependency on speed binning by employing a more cost-effective, structural, at-speed test approach. With this question in mind, the authors show that speed binning results obtained from structural testing of selected critical paths correlates closely with results from functional testing. The authors then offer a formula that relates critical-path testing frequency to system-operation frequency. Although these results might be design and frequency dependent, this work demonstrates the possibility of replacing functional testing with structural testing in speed binning. It should inspire future studies to delineate a clear boundary between the applications of the two approaches.

Finally, Bob Madge and Brady Benware of LSI Logic and Rob Daasch of Portland State University tackle the effectiveness of structured delay tests for defect detection across a wide spectrum of operating conditions. It is common to apply most IC tests at varying voltages and temperatures, and to sometimes modulate the frequency as well. All these variations, particularly frequency modulation, can have an unknown effect on the quality of the overall test results. Although maximizing outgoing quality is desirable, doing so with minimal yield loss is equally important. The authors detail their approach for test generation and application on silicon, comparing defect detection for patterns from different test generation strategies. They apply patterns at various operating frequencies to empirically derive a relationship between test frequency and defect coverage. They also make several observations related to yield impact, overkill rate, and failure analysis.

THESE SIX ARTICLES provide an excellent summary of the state of the art in at-speed testing. We hope you enjoy this special issue. ■

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